DESIGN AND ANALYSIS OF IMPEDANCE-MATCHING AND DICKSON-VOLTAGE-MULTIPLIER FOR 915-MHZ RF ENERGY/HARVESTING SYSTEM

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Master Thesis
Prepared as

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I certify that in my opinion the presented thesis that has been submitted by Tiba Hussein GATEA titled ‘’DESIGN AND ANALYSIS OF IMPEDANCE-MATCHING AND DICKSON-VOLTAGE-MULTIPLIER FOR 915-MHZ RF ENERGY/HARVESTING SYSTEM” is fully adequate in scope and in quality as a thesis for the degree of Master of Science.

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Tiba Hussein GATEA

ÖZET

Yüksek Lisans Tezi

915 MhZ ENERJİ HASAT SİSTEMİ İÇİN EMPEDANS EŞLEŞTİRME VE DİCKSON GERİLİM ÇARPANININ TASARIMI VE ANALİZİ

Tiba Hussein GATEA

Karabük Üniversitesi
Mühendislik Fakültesi
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Dünya sürdürülebilir ve yenilenebilir enerji kaynaklarına doğru kaymaya devam ederken, RF enerji toplama sistemleri, ortamdaki radyo frekans dalgalarını kullanılabilir elektrik gücüne dönüştürerek düşük güçlü elektronik cihazlara güç sağlamak için umut verici bir çözüm olarak popülerlik kazanıyor. Bu tez, -40 dBm ile 40 dBm arasındaki giriş gücü için RF enerji toplama parametreleri ile çıkış DC voltajı arasındaki ilişkiyi analiz eder ve araştırır. (L, T ve π) eşleştirme ağları gibi Dickson voltaj çarpanı aşamalarını (DVÇ'ler) tasarlamak için üç tür eşleştirme empedans ağı kullanılmıştır. Bu çalışmada 20 ila 2500 kΩ yük direnci aralığı için DVM'nin tasarımı ve uygulaması yapılmıştır. Bu tez, alternatif empedans eşleştirme, empedans ağlarının verimliliği ve çıkış DC voltajını nasıl etkilediğini inceler. DVM devrelerini tasarlamak için üç tip Schottky diyot modeli kullanılmıştır: HSMS-2852, HSMS-2822 ve HSMS-2860. Her bir simülasyonu gerçekleştirmek için Gelişmiş Tasarım Sistemi (GTS) 2021 ortamı kullanılmıştır. Tasarımda kullanılan Endüstriyel, Bilimsel ve Tıbbi Radyo

Bandı (ISM bandı) hedef frekansı 915 MHz'dir. Düşük seviyeli giriş gücünde, simülasyon sonuçları, eşleştirmeli DVÇ devresi tasarımının, eşleştirmesiz DVÇ devresinden daha verimli olduğunu göstermiştir. Ek olarak simülasyon sonuçları, düşük yük kullanımının hasat devresinin verimliliğini artırdığını göstermektedir. Ayrıca HSMS-2852 Schottky diyot modelleri, HSMS-2822 modellerinden ve HSMS-2860 modellerinden daha verimlidir. Ayrıca HSMS-2860, en düşük ileri voltaj düşüşüne ve en yüksek ters voltaj değerine sahiptir, bu da onu bir Dickson voltaj çarpanı için en verimli seçim haline getirir. Ayrıca, tüm tasarımlar verimlilik düzeyine bağlı olduğundan, eşleştirme devresi olan toplama sistemi, düşük giriş gücü için eşleştirme devresi olmayan toplama sistemine göre daha avantajlıdır. Bu nedenle, bu tezdeki tüm simülasyon bölümleri için hem voltaj hem de verim için karşılaştırma sonucu ve veri analizi ayrıntılı olarak yapılmıştır.

Anahtar Sözcükler : RF enerji hasadı, Dickson voltaj çarpanı (DVM), Uyumlu empedans, Kalite faktörü ve Gelişmiş Tasarım Sistemi (GTS)

Bilim Kodu : 90513

ABSTRACT

M. Sc. Thesis

DESIGN AND ANALYSIS OF IMPEDANCE MATCHING AND DICKSON VOLTAGE MULTIPLIER FOR 915 MHZ RF ENERGY HARVESTING SYSTEM

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Department of Electrical and Electronics Engineering

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As the world continues to shift towards sustainable and renewable energy sources, RFEH systems are gaining popularity as a promising solution for providing power to low-power electronic devices by converting ambient radio frequency waves into usable electrical power. This thesis analysis and investigates the relationship between RFEH parameters and the DC output voltage for input power from -40 dBm to 40 dBm. Three types of matching impedance networks have been used to design Dickson voltage multipliers stages (DVMs) such as (L, T, and π) matching networks. The design and implementation of DVM in this study for a range of load resistances from 20 to 2500 kΩ. To examine how alternative impedance matching impedance networks affect efficiency and output DC voltage. To design the DVM circuits, three types of Schottky diode models have been used: HSMS-2852, HSMS-2822, and HSMS-2860.

The Advance Design System (ADS) 2021 environmental has been utilized to perform every simulation.

The Industrial, Scientific, and Medical Radio Band (ISM) selected frequency used in the suggested design is 915 MHz. At low-level input power, the simulation results indicated that the DVM circuit design with matching was more efficient than the DVM circuit without matching. Additionally, the simulation results demonstrate that low load usage boosts the harvesting circuit's efficiency. Furthermore, HSMS-2852 Schottky diode models are more efficient than HSMS-2822 models and HSMS-2860. Besides, The HSMS-2860 has the lowest forward voltage drop and the highest reverse voltage rating, which makes it the most efficient choice for a Dickson voltage multiplier. Moreover, the harvesting system with a matching circuit benefits the system without a matching circuit for low input power because all designs depend on the efficiency level. Hence, the comparison result and data analysis for both voltage and efficiency has been done in detail for all simulation parts in this thesis.

Key Word: RF-energy harvesting, Dickson voltage multiplier (DVM), Matching impedance, Quality factor, Advanced Design System (ADS).

Science Code: 90513

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INDEX OF ICONS AND ABBREVIATIONS

ICONS

μW : Microwatt

KΩ : Kilo ohm

Ω : ohm

AC : alternating current

DC : direct current

V_{br} : The reverse breakdown voltage

V_f : The forward voltage drops

C_d : capacitance

C_d : inductance

P_d : maximum power dissipation

I_f : maximum forward current

T_{max} : maximum operating temperature

T_{min} : minimum operating temperature

f : the frequency of operation

X_l : the desired inductive reactance

X_c : the desired capacitive reactance

Z_l : the load impedance

P_{DC} : the output-power in DC

P_{AC} : the input power in AC

P_{load} : the output-power to the load

P_{source}: the input power from the source

ABBREVIATIONS

ADS : Advanced Design System
GSM : Global System for Mobile
GHz : Gigahertz
MHz : Megahertz
ISM : The industrial, scientific and medical (ISM) radio bands
RF : Radio Frequency
RFID : Radio Frequency Identification
UHF : Ultra-high frequency.
UMTS : Universal Mobile Telecommunications System
VSWR : Voltage Standing Wave Ratio
WiFi : Wireless Fidelity, wireless internet
WiMAX : Worldwide Interoperability for Microwave Access.
WLAN : Wireless Local Area Network
WSNs : Wireless Sensor Networks
SBD : Schottky Barrier Diodes
STD : Schottky Tunnel Diodes
MIS : Schottky Metal-Insulator-Semiconductor
MOS : Schottky Metal-Oxide-Semiconductor
SiC : Schottky Silicon-Carbide (SiC) Diodes
RFEH : Radio Frequencies Energy Harvesting

PART 1

INTRODUCTION

Today, electromagnetic waves of many different frequencies are constantly present in the environment, especially in living spaces. This shows that electromagnetic waves are present in almost every environment. RFEH is the method of getting the amount of energy needed from environmental RF signal sources [1].

In parallel with the development of the modern world and technology, the devices used today are also developing. The development of devices increases the need for energy resources. Energy harvesting circuits also offer instant and continuous solutions in providing the power and energy needed by electronic circuits and devices [2].

Energy harvesting is a very popular process today. Energy harvesting circuits have become quite common instead of batteries and similar energy storage cells. Both academic and industrial studies have begun to benefit significantly from energy harvesting methods in supplying the energy needed by electronic devices [3]. Because the batteries have started to become useless because they are both heavy and bulky and take up a lot of space in terms of volume, it both needs recharging in a short time, and the batteries have a limited usage time. On the other hand, electromagnetic waves and communication signals in the environment are continuous. In this respect, energy harvesting will provide advantages in many ways [4].

The process of obtaining direct current and voltage from the communication signals in the environment RFEH is based on harvesting the continuously emitted energy. In this respect, it can be said that it is a continuous source of energy [3]. This method can be implemented with low-cost and light-circuit elements. The most significant disadvantage of this method is the low power density it can convert. In addition, this power density decreases with the distance from the sources.

Considering the advantages and disadvantages of RFEH circuits, their usability should be evaluated despite such low power density and varying according to the distance from the communication signal sources.

The energy/harvesting circuits in the literature are divided into two near-field and far-field energy harvesting circuits according to their energy intake distances. Near-field energy applications are mostly recommended for biomedical applications and wearable technologies. Example of projected far-field energy harvesting applications electricity. Power transmission studies at distances not close to the source and for remote sensing applications [3].

The RFEH process includes transferring the DC power obtained with the help of the received matching and rectification circuits to the power supply input of the device to be operated [5].

The absence or minimum of reflection in a microwave circuit indicates impedance matching. The signal received from the receiver (antenna, etc.) is reflected, standing wave, etc., before the rectifier comes into operation. If the signal frequency is the same as the matching frequency, the reflection level decreases, and the signal rectifier, which carries more power, is activated [5]. The matching layer is essential so that a received electromagnetic wave does not suffer from distortion and attenuation. The point to be reached in the RFEH process is to realize the optimum design by making microstrip antenna designs and applications covering a wider frequency band and having different geometric shapes [6].

By using these properties of microstrip antennas, microstrip antenna design has been tried in RF-energy harvesting, which is the subject of the thesis. Parameters such as patch shape, size, and resonance frequencies, dielectric values of the antenna are essential, and these features can change the parameters of the antenna [7]. Therefore, it can also affect the performance of the antenna. As a result of the parametric analyses made in the simulation environment, the parameters giving the best results were determined, and the antennas were produced [8].

Today, electromagnetic waves of many different frequencies are constantly present in the environment, especially in living spaces. This shows that electromagnetic waves are present in almost every environment. For example, mobile phone signals emitted from base stations are GSM 1800, EDGE, 3G, 4.5G etc. for wireless internet from base stations. The powers carried by the signals emitted from the communication systems, such communication systems, or the powers of the signals from the ISM band emitted from the wireless modems inside the buildings, are examples of instant electromagnetic waves in the environment. In addition, digital television broadcasts (DVB-T) and FM radio waves are among these signals. When attention is paid, electromagnetic waves in the environment have many different frequencies. In addition, it can be in many different power ranges according to its usage areas [9].

In general, energy harvesting circuits are based on converting the energy in the environment into direct current and voltage. There are also energy harvesting methods in the literature by converting different types of energy from RF. These primary energy harvesting techniques can be considered in the clean energy class; solar (solar), thermal (thermal), and vibrational (piezzo) energies [5].

Considering the usage areas and conditions of energy harvesting techniques, RFEH has advantages and disadvantages compared to the other three techniques. The power density obtained from solar energy is relatively high. However, this type of energy is not continuous, as the duration of benefiting from the sun varies according to the season and location [11]. Therefore, either the solar energy will be consumed instantly or used together with the storage units. On the other hand, its high energy density makes solar energy an irrefutable position among the energy harvesting processes [5].

In the literature, energy harvesting circuits are divided into near-field and far-field energy harvesting circuits according to their energy intake distances. Near-field energy harvesting applications are mostly recommended for biomedical and wearable technologies [8,10]. For example, the first application that comes to mind is the pacemaker's power transmission circuit application. Many similar application areas can be considered in the context of 'quality life' and 'advancement in medicine'. In addition, sensors on a garment we wear may be powered by energy harvesting circuits.

Examples of predicted far-field energy harvesting applications are power transfer studies at distances not close to the electricity source and remote sensing applications [11]. In the literature, studies on far-field applications of stand-alone RF-energy circuits have begun to concentrate [12]. Some far-field applications operate at low currents and voltages and consume low power; low-power sensor applications, internet of things (IoT) applications, microprocessor-based sensor platforms, and low-power voluntary circuits [11,13].

One of the literature studies that has become widespread is using energy harvesting circuits together. Recently, 'hybrid energy harvesting circuits' have also started to be studied. Using two or more energy harvesting techniques (for example, solar energy and RF energy) with the opportunities provided by suitable power management units is considered commercially available in the future [5].

1.1. ENERGY HARVESTING WITH RADIO FREQUENCIES

Wireless sensor networks are everywhere, from factories to cars, smart buildings to the human body. It is said that with the rapid developments in IoT and new wireless technologies, wireless sensor networks will be an integral part of our lives. These networks, which often consist of thousands of nodes, are spread over a wide area [14,15]. Each node forming the network receives its power from batteries. A node's survival and data transmission in the network is as long as the batteries allow. A sensor node with a dead battery cannot transmit data to the center [16]. If other nodes transmit data through this node, the problem gets bigger. It is necessary to observe whether the network nodes are working and replace the dead batteries, if any. However, in some circumstances, replacing the battery is a complicated process. For example, it is not easy to replace a sensor's battery attached to bridge piers and detect cracks in concrete. In addition, the destruction of discharged batteries is another process that will cause environmental problems [5,17]. All these problems can be examples of obstacles to the rapid spread of wireless sensor networks. In this regard, energy harvesting can be considered an alternative to batteries. Energy harvesting is efficiently converting existing energy resources and making them usable. Energy harvesters take vibration, temperature, heat, light, and RF energy into proper form and store it [18].

RF-energy harvesters harvest using airborne RF signals. These signals are mostly radiated from base stations, TV transmitters, mobile phones, and modems. The difference between RF-energy harvesters from wireless power transmission systems is that harvester systems can operate at very low power. For this reason, harvesters need to work as efficiently as possible. Figure 1.1 shows a standard RF-energy harvester system.

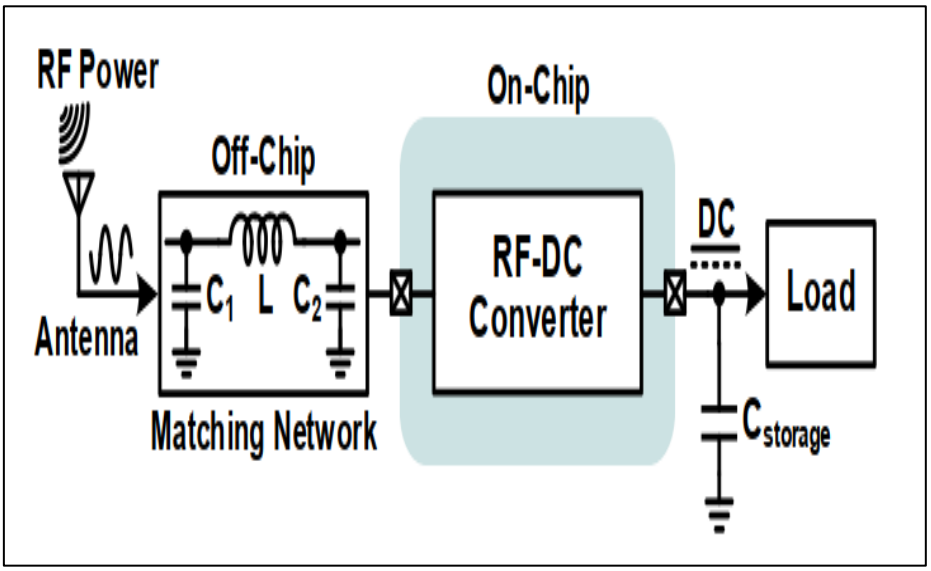


Figure 1.1. The energy harvesting system diagram of Radio Frequency (RF) [18].

As seen in Figure 1, the first element, which is the key of the system, is the antenna. The antenna is a passive element that collects RF-energy in the environment. Harmonic signals are formed at the end of the RF-DC rectification process. The reflection of harmonics back to the antenna reduces its performance and the system's efficiency. The rectifier is the most crucial element that makes the RF-DC conversion and determines the rectifier antenna efficiency [18].

Rectifiers consist of transistors or diodes. Diode rectifiers are used in RFEH rectifier antennas. Schottky diodes are preferred for rectifying high-frequency signals. Rectifiers are designed on different surfaces in line with the requirements of the system [19]. If it is desired to operate an electronic device with the energy obtained from the rectifier antennas, DC-DC boost converters are required [6,7].

The DC-DC boost converter increases the low output-voltage to the functional level. Batteries or supercapacitors are used when the output-power is not used immediately and is wanted to be stored. Although supercapacitors are not an alternative to batteries, their storage capacities and usage purposes differ. Although supercapacitors can be charged and discharged thousands of times, their performance suffers very little. Batteries allow longer energy retention. The power and energies of various power storage units are given in Figure 3.2.

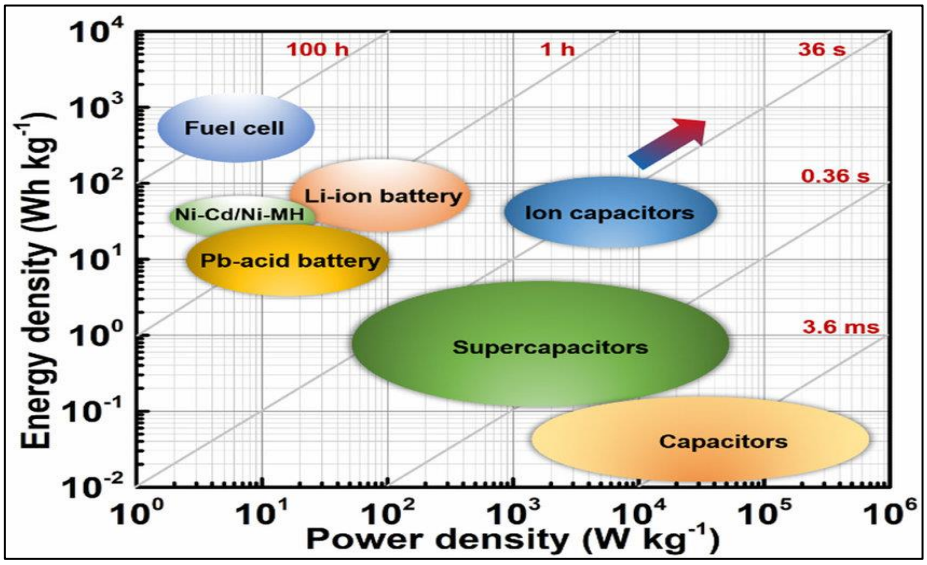


Figure 1.2. The density of several source energy storage [20]

The absence or minimum of reflection in a microwave circuit indicates impedance matching. The signal received from the receiver (antenna, etc.) is reflected, standing wave, etc., before the rectifier comes into operation. If the signal frequency is the same as the matching frequency, the reflection level decreases, and the signal rectifier, which carries more power, is activated [21].

1.2. CONCEPTS IN ENERGY HARVESTING

This section gives the concepts and definitions that constitute the theoretical infrastructure of energy harvesting studies. The relationship between energy and power and the location of the maximum power transfer (MPT) problem in energy harvesting has been evaluated.

A primary energy harvesting circuit consists of rectification, matching, and transmission circuits. Theoretical calculations of input and output parameters in rectifier circuit design are given in this section. These parameters are input power, output voltage, output power, load resistance, and power conversion efficiency.

An RFEH circuit captures the communication signals emitted in the environment (air), converts them to direct current and voltage, and transfers them to the device to be used. For this to happen, the reflection must be minimum in that communication band of the energy harvesting circuit. Absence or low reflection is a measure of impedance matching. This section gives definitions of impedance matching, reflection, transmission and bandwidth, and basic calculations in energy harvesting applications.

Table 1.1. The values and types of energy harvesting sources [21].

Source	The power	Harvestedin Power	Advantages	Disadvantages
Light				
Indoor	0.1 mW/cm2	10 W/cm^2	High power density Mature	Not availablealways Required exposureto light costly
Outdoor	100 mW/cm^2	10 mW/cm^2		
Vibration / Motion				
Human	0.5 m at 1 Hz		Implantable High efficiency	Not availablealways Material physical limitation
	1 m/s^2 at 50 Hz	4 W / cm^2		
Machine	1m at 5 Hz			
	10 m/s^2 at 1 kHz	100 W/cm^2		
Thermal				
Human	20 mW/cm^2	30 W/cm^2	High power density Implantable	Not availablealways Overflow heat
Machine	100 mW /cm^2	1-10 mW/cm^2		
RF				
GSM	0.3 W/cm^2	0.1 W/cm^2	Always available Implantable	Low density Efficiency inversely proportional to distance

[21,22]. One of GSM's key characteristics is a circuit-switched architecture, which creates a dedicated connection between the mobile phone and the network for the length of a conversation or data session. Unlike other mobile communication protocols, including CDMA (Code Division Multiple Access), which employ a packet-switched design, this architecture is distinct [21,23]. The SIM card (Subscriber Identity

Module), a tiny chip card put into a mobile phone and holds a subscriber's personal information, is also standardized by GSM. Users may do this without updating their phone number or personal information, making it simple to transition between multiple mobile phones [21–23]

Due to GSM's widespread acceptance and success, the third-generation (3G) mobile communication standard knowen as UMTS "Universal-Mobile-Telecommunications-System", which is still in use today, was created as a result. The usage of 900 and 1800 MHz worldwide is seen in Figure 1.3.

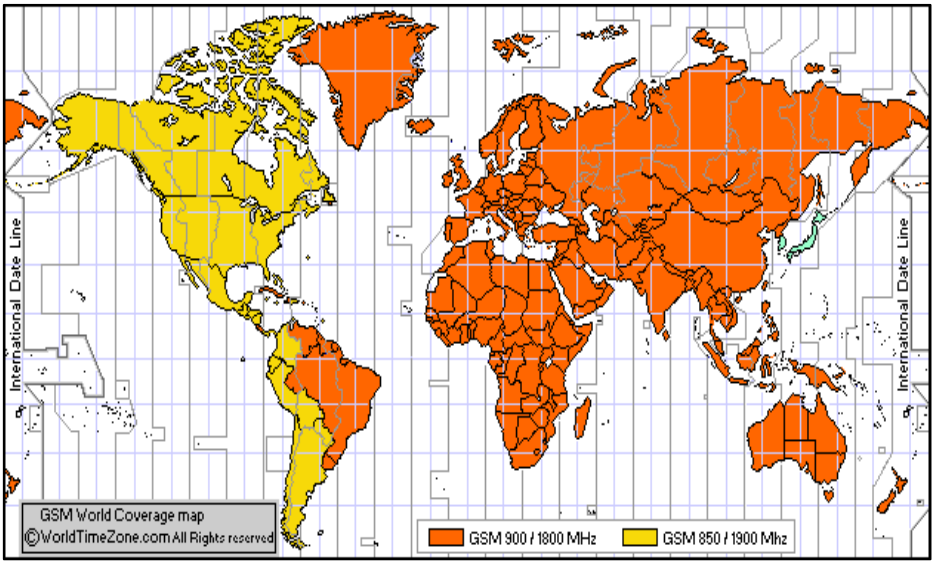


Figure 1.3. GSM (Groupe Special Mobile) [22]

1.3. THE SELECTED FREQUENCY 915 MHZ

915 MHz is vital for several reasons. One of the main reasons is that it is a license-free frequency band, which means that it can be used without a license in many countries. This makes it a popular choice for low-power wireless devices, such as wireless sensor networks and"radio frequency identification" (RFID) systems [12].

Another reason why 915 MHz is essential is that it is considered a "sweet spot" for wireless communication. The propagation characteristics of the 915 MHz band make it suitable for use in environments where line-of-sight communication is not possible,

such as in urban environments or around obstacles [12]. This makes it an ideal frequency band for industrial, scientific, and medical (ISM) applications, where communication needs to be maintained even in challenging environments [24].

Additionally, in the ISM band, it is less crowded than other ISM bands, and thus it has less interference. This makes it a good choice for applications requiring high reliability and low error rates, such as wireless sensor networks and RFID systems [12].

Finally, it's also worth mentioning that the 915 MHz frequency band is widely used in the Americas, Australia and New Zealand, Turkey, Iraq, and several Middle east countries, which means that devices operating on this frequency band can be used in those countries without the need for additional certifications or approvals [24].

As shown in Figure 1.4, In GSM-900, data is sent in two directions: uplink from the mobile station to the base station (890 to 915 MHz) and downlink from the base station to the mobile station (935 to 960 MHz). (890 MHz to 935 MHz) Duplex spacing of 45 MHz is employed. In comparison to GSM-1800, GSM-900 has twice the coverage and suffers from lower propagation losses. On the GSM-900 bands, only Globe, Smart, and Islacom primarily acquired frequency assignments. [24]. Table 1.4 represent the 915 MHZ frequency band used.

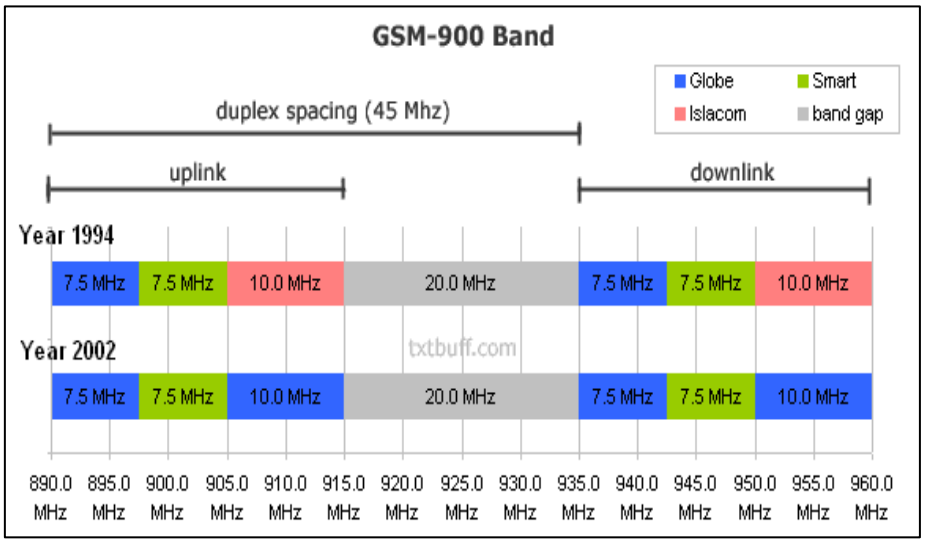


Figure 1.4. Uplink and downlink of GSM-900 band [24].

Table 1.2. The 915 MHZ frequency band was used [24].

Transporter	Attaining a Frequency	Bandwidth
Globe-system	(890 to 897.5) MHz (93 to 942.5) MHz	7.5 MHz
Smart-system	(897.5 to 905) MHz (942.5 to 950 MHz	7.5 MHz
Globe-system	(905 to 915) MHz (950 to 960) MHz "Islacom once owned this property."	10 MHz

For several reasons, the 915 MHz frequency band is important for RFEH in Turkey and Iraq [24].

- Firstly, the 915 MHz frequency band is one of the ISM bands allocated for unlicensed use in Turkey, which means it can be used without needing a license. This makes it a popular choice for wireless energy harvesting systems, as it eliminates the need to obtain a license and reduces costs.
- Secondly, the 915 MHz frequency band is less crowded than other ISM bands in Turkey, which means it has less interference and higher reliability for wireless energy harvesting systems.
- Thirdly, the 915 MHz frequency band can penetrate through obstacles and can cover a large area, making it ideal for wireless energy harvesting applications where the energy source and the energy receiver need to be separated by some distance or placed in different locations.
- Finally, the 915 MHz frequency band is widely used in wireless applications in Turkey. Thus, devices operating on this frequency band can be used in Turkey without additional certifications or approvals, making it a practical option for wireless energy harvesting systems.

1.4. THE RECTIFIER

The Recttifire is a voltage multiplier circuit. It is a device used to convert alternating current (AC) to direct current (DC) by multiplying the input signal's voltage. This is useful in various applications, including radio frequency (RF) energy harvesting,

where the circuit converts the weak, high-frequency signals from RF sources into usable DC power.

The basic principle of a voltage multiplier circuit is to take a single AC waveform and convert it into multiple DC-output voltage levels by using a series of diodes and capacitors. The diodes are used to rectify the AC-waveform and convert it into a pulsating DC-signal, while the capacitors are used to smooth out the pulsations and provide a steady DC-output.

There are several types of voltage multiplier circuits, each with unique characteristics and advantages. One of the most common types is the diode-capacitor voltage multiplier, also known as a "charge pump," which uses a series of diodes and capacitors to generate a high DC voltage from a lower AC input. Another popular type is the diode-resistor voltage multiplier, which combines diodes and resistors to generate a lower DC voltage from a higher AC input [9].

One of the main advantages of voltage multiplier circuits is their ability to produce high DC voltage outputs from low AC inputs. This makes them ideal for RFEH applications, where the input signals are typically weak and high-frequency. In these applications, the circuit can be used to convert the weak RF signals into usable DC-power, which can then be stored in a battery or used to power other electronic devices.

Another advantage of voltage multiplier circuits is their high efficiency and low cost. Since they do not require moving parts or complex mechanical components, they can be manufactured relatively cheaply and have a long lifespan. Additionally, they are highly reliable, making them ideal for use in remote or harsh environments.

In conclusion, voltage multiplier circuits, also known as rectifiers, are essential to RF-energy harvesting. They convert weak and high-frequency signals into usable DC power. They come in different types, such as diode-capacitor voltage multipliers and diode-resistor voltage multipliers, each with its characteristics and advantages. They are efficient, low-cost, and reliable, making them suitable for remote or harsh

environments. Figure 1.5 below represents the simple rectifier circuit diagram in RF-energy harvesting.

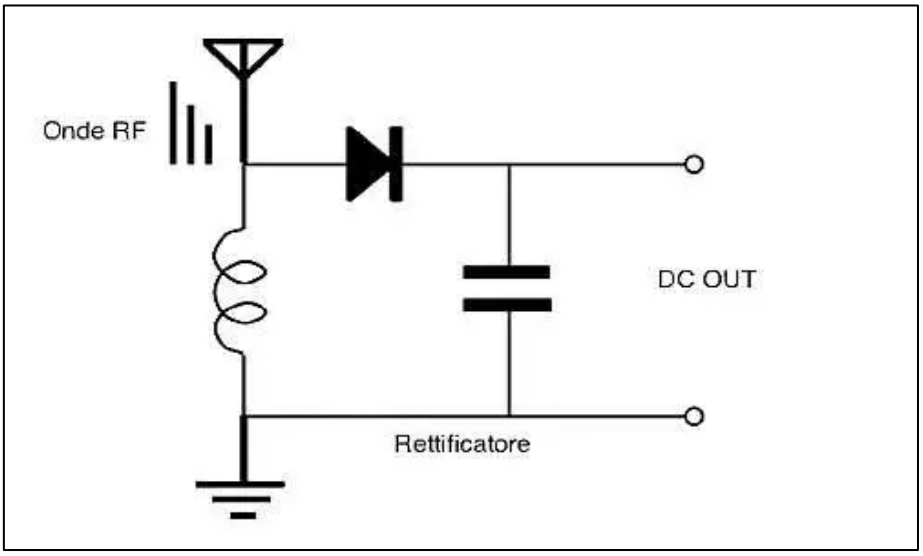


Figure 1.5. The simple rectifier circuit diagram in RF-energy harvesting.

1.5 IMPEDANCE-MATCHING-CIRCUIT

The impedance matching circuit in RF-energy harvesting system is used to optimize energy transfer from the RF signal source to the load (such as a battery or storage device). The circuit is created to maximize energy transmission efficiency and reduce reflections by matching the impedance of the energy source to the impedance of the load [10]. This can be done using various circuit components, such as transformers, inductors, and capacitors. The specific design of the impedance-matching circuit will depend on the particular frequencies and power levels used in the system [10,25]. Figure 1.6 below represents the Matching impedance network strategies used in RF energy harvesting systems.

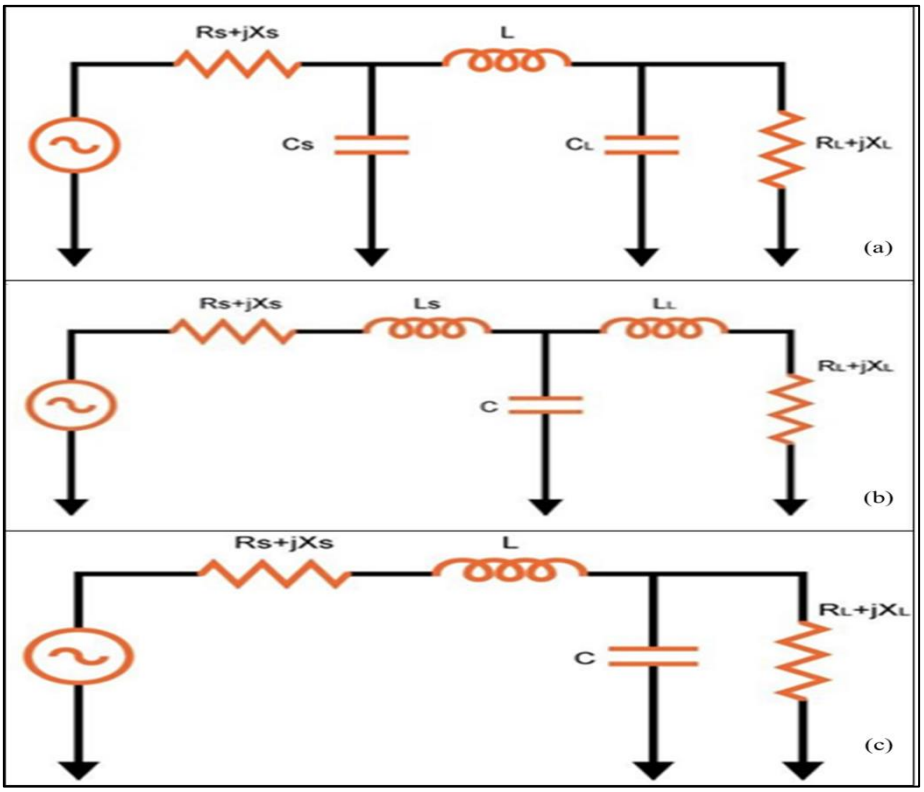


Figure 1.6. The designs of the matching networks (a) π, (b) T, and (c) L [25].

1.6. SCOPE AND-OBJECTIVES

This thesis aims to study, design and analyze the Dickson voltage multiplier circuit, which is used to harvest the frequencies of radio waves with a frequency of 915 megahertz. Also, a study of the effect of the impedance circuit on the output values of the amplifier circuit in order to reach the highest possible matching value with the antenna, which will lead to high-value outputs for each of the power, current, voltage, and circuit efficiency through the proposed frequencies that are received. Also, the proposed impedance circuit designs will be addressed to reach the highest matching value. In addition, a study of the quality factor on impedance circuits and their differences in the design of the amplifier and a comparison of the results. Therefore, this thesis will crystallize the analytical results of each studied and designed case.

1.7. THE OUTLINES AND THESIS DECLARATION

There are five parts in this thesis:

- Part 1: Explain the introduction to the RFEH and the other type of harvesting. Besides, describing the selected frequency and the main component of the RFEH system.
- Part 2: The literature review about harvesting systems in 915 Mhz. Besides, the related works of the DVM rectifier and the matching impedance network designs.
- Part 3: Defining the characteristics of the component utilized in this thesis while describing the approach of the suggested designs.
- Part 4: Explain the simulation, analysis, and result of designed circuits and the quality factor of each circuit.
- Part 5: Conclusion and discussion of this study.

PART 2

LITERATURE REVIEW

RFEH extracts energy from radio frequency (RF) signals and converts it into usable electrical energy. One of the most commonly used frequency bands is the 915 MHz band, allocated for industrial, scientific, and medical (ISM) applications [1]. Most recently, there has been a growing interest in using RF energy harvesting for various wireless sensors and IoT applications. The 915 MHz band is particularly attractive for these applications due to its relatively high-power levels and long-range propagation characteristics [2].

Several investigations have been done on the topic of RF energy/harvesting in the 915 MHz range. One of the critical challenges in this frequency range is to design efficient and compact rectifiers that can convert RF energy into usable DC power. Researchers have proposed a variety of rectifier topologies, such as single-diode, double-diode, and active rectifiers, to improve energy conversion efficiency [1,14]. Another important aspect of RF energy harvesting is the design of antennas and impedance-matching circuits. Researchers have investigated different antenna types, such as dipoles, loops, and patch antennas, to optimize the energy transfer between the RF source and the energy harvester. Additionally, impedance-matching circuits have improved energy transfer efficiency and reduced reflections [16,26].

In addition to the technical challenges, regulatory and standardization issues need to be considered for RFEH in the 915 MHz bands. Due to the ISM nature of this band, the use of RFEH may be subject to different regulations and standards depending on the location and application. [16,26].

Overall, RFEH in the 915 MHz band has the potential to provide a reliable and efficient source of energy for a wide range of wireless sensor and IoT applications. However,

further research is needed to address the technical and regulatory challenges and to develop more efficient and compact energy harvesting solutions.

2.1. RELATED WORK

RFEH extracts energy from radio frequency (RF) signals and converts it into usable electrical energy. One of the most commonly used frequency bands for RFEH is the 915 MHz band, allocated for industrial, scientific, and medical (ISM) applications [10].

Recently, there has been a growing interest in using RFEH for various wireless sensors and IoT applications. The 915 MHz band is particularly attractive for these applications due to its relatively high-power levels and long-range propagation characteristics.

Several studies have been conducted on RFEH in the 915 MHz band. One of the critical challenges in this frequency range is to design efficient and compact rectifiers that can convert RF energy into usable DC power. Researchers have proposed a variety of rectifier topologies, such as single-diode, double-diode, and active rectifiers, to improve energy conversion efficiency [25].

Andrea Ballo. et al., in 2022, provided that this paper accurately analyzes the Dickson-Voltage-Multiplier (DVM) dynamic behavior, including the charge transfer limits. The findings demonstrate that the DVM is fundamentally inefficient in settling time and power conversion when operating in the "Fast-Switching-Limit" (FSL). With an inaccuracy of less than 14%, simulation results using SPICE and a 0.13-m CMOS technology support the theoretical analysis, while simulation results using LTSPICE and a 0.13-m CMOS technology support the prediction of dynamic behavior with an accuracy of 5.5% [2].

Kei Eguchi, et al. 2021 proposed a new system in the paper. The validity of the proposed multiplier is confirmed through "simulation program with integrated circuit emphasis" (SPICE) simulations and experiments. The SPICE simulations and

investigations reveal that the proposed multiplier outperforms the conventional (HCWDM). For the design of shockwave non-thermal food processing systems, a novel high-speed bipolar voltage multiplier is presented in this paper, as explained below in Figure 2.1. Unlike conventional high voltage multipliers, the proposed voltage multiplier has bipolar topology employing hybrid Cockcroft-Walton/Dickson-multipliers (HCWDMs), where the bipolar is driven by a driver circuit generating high-speed rectangular pulses [4].

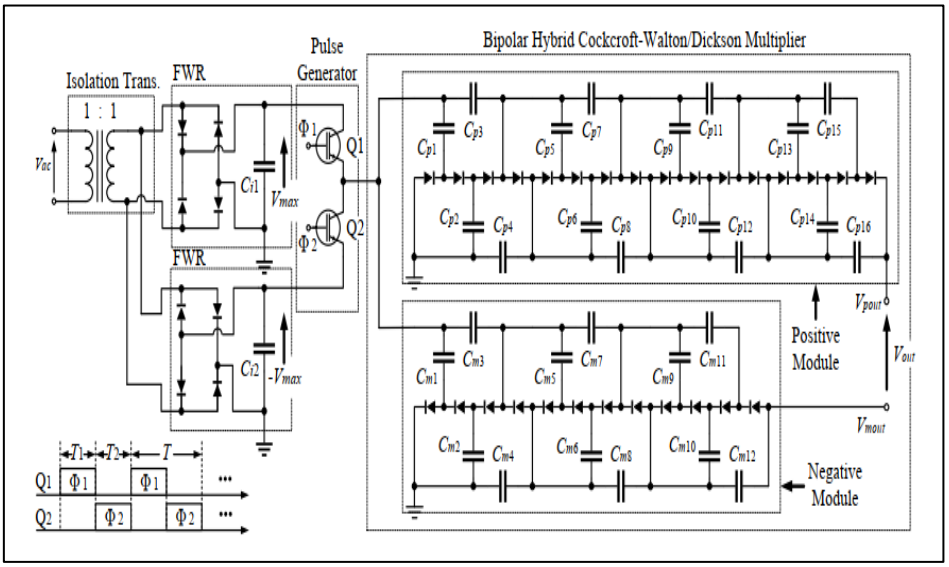


Figure 2.1. Proposed high voltage multiplier [4].

Sittilin Salleh, et al. in 2021 A new study is being suggested that focuses on designing and simulating a voltage doubler rectifier circuit running at 2.45 GHz, optimized using the Schottky diode HSMS 286 B. A multi-stage rectifier produces maximum conversion from AC to DC, with a maximum power conversion efficiency of 73.13%, as shown below in Figure 2.2 [3].

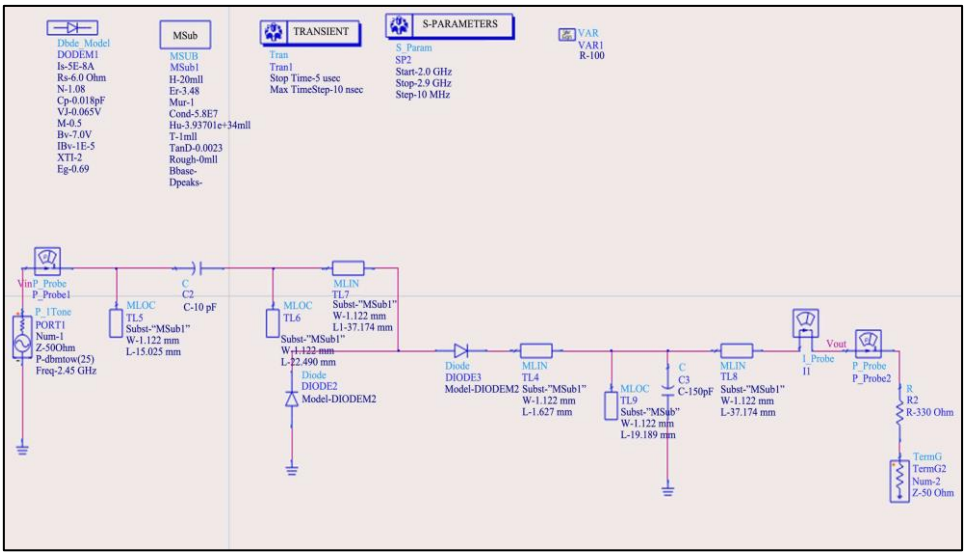


Figure 2.2. The voltage doubler rectifier layout circuit by ADS program [3].

Filiz SARI and Yunus UZUN in 2019 have presented research for "Villard, Dickson, and Greinacher rectifiers". According to the set inputs of the harvester-designed rectifier by ADS, as shown below in Figure 2.3, the voltage multipliers are evaluated without impedance matching and substrate materials to determine the most effective type. The findings demonstrate the significance of load resistance in assessing high efficiency. For instance, for a Dickson voltage multiplier operating at a 100 MHz input frequency, efficiency variances between 2 and 20 kΩ are as high as 33%. The Greinacher voltage multiplier is the best option to achieve high efficiency for low-frequency applications, as demonstrated by the study, which also reflects the importance of load resistance, input frequency, and input power [25].

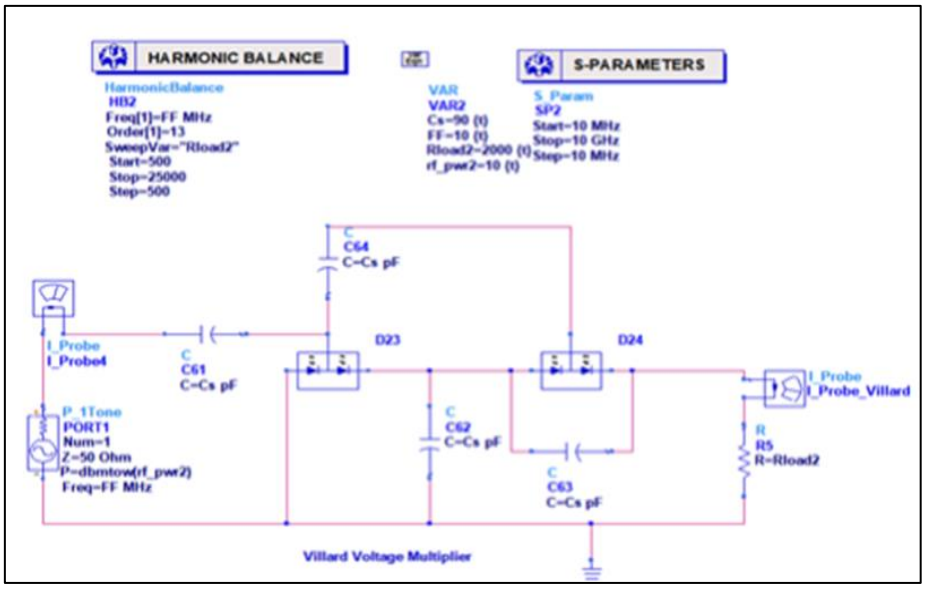


Figure 2.3. Villard VM circuits from ADS software [25].

Musaab Mohammed AL-Azawy and Filiz Sari 2019 presented a paper that gives RFEH values for input powers between -35 dBm and 25 dBm that rely on output DC voltage and efficiency. Dickson voltage multipliers (DVMs) with multiple stages ranging from two to six stages are created and used with varying load resistance and matching topologies, including L, T, and π matching. Besides, Simulation findings show that the DVM circuit design with matching generates high efficiency and high output DC voltage compared to the DVM circuit without matching for low input power. The HSMS-2852 Schottky diode modal performs better in low input power than the HSMS-2822 Schottky modal [17].

An article illustrating a unique analytical model for the voltage multiplier rectifier at 900 MHz was published in 2018 by Esraa Mousa Ali, et al. The model suggests a method for determining the rectifying circuits' output characteristics regarding two key variables: voltage and current. A Schottky diode called the HSMS 285C was employed in the seven-stage Dickson voltage multiplier rectifier that makes up the design. The system was constructed and tested in accordance with the input power range of $(1 \times 10^{-5} - 1 \times 10^{-1})\ W$. According to experimental findings, an output voltage of 5.45 V and a 1.26 × 10−5 A current are attained at 10 dBm with a 10 kΩ load, yielding a 37.82% efficiency [27]. Figure 2.4 shows The linearized model of the Dickson voltage multiplier during positive peak for the seven stages. Figure 2.5 shows the

design of the seven stages of the Dickson voltage multiplier circuit [27]. The voltage waveforms for the Dickson voltage multiplier circuit with and without matching are explained in Figure 2.6 below.

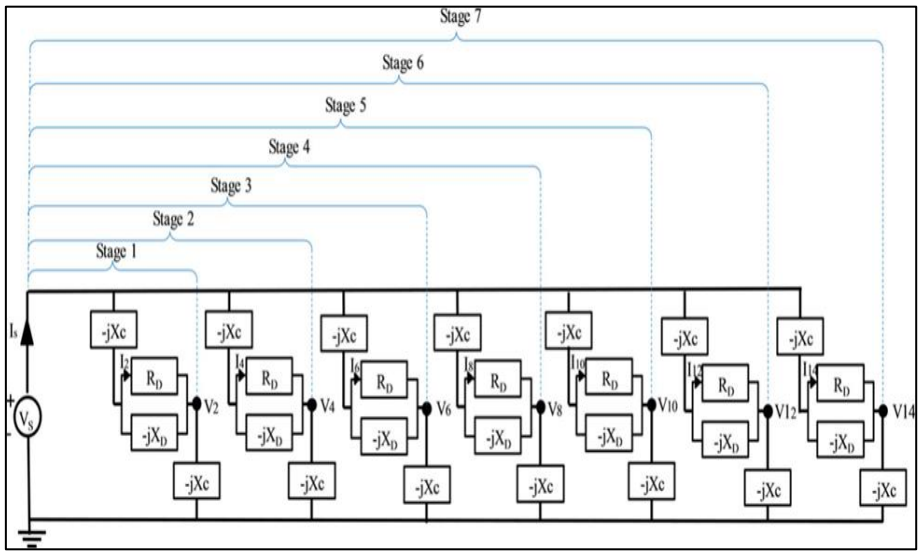


Figure 2.4. The DVM's linearized model for the seven stages of a positive peak [27].

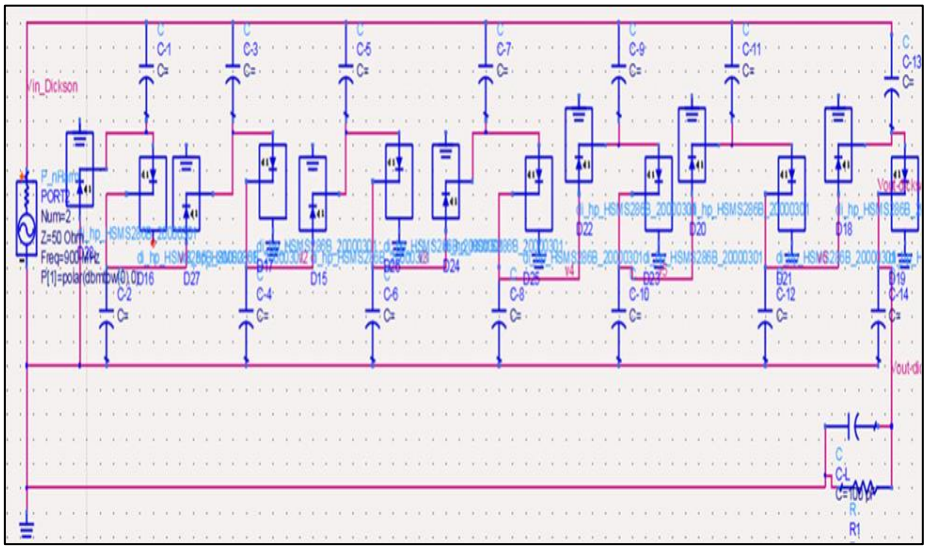


Figure 2.5. The DVM's stages are designed by the ADS program [27].

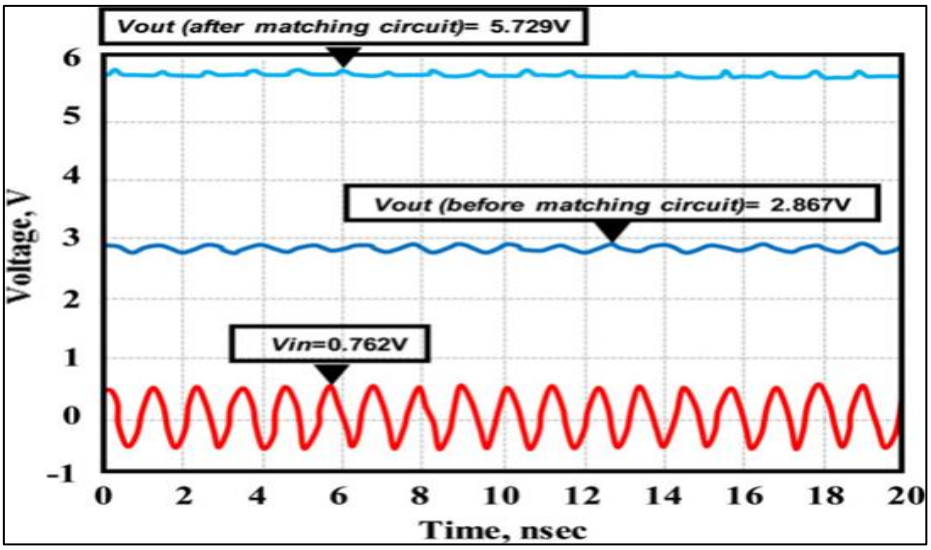


Figure 2.6. Waveforms of the voltage for the DVM circuit with and without matching [27].

Asma Anika Shahabuddin, et al. in 2018. They focus on the design of a five-stage voltage multiplier with a type-matching circuit for an RFEH system using input power from the GSM-900 band presented in the research paper. After the design was completed using the ADS simulator, the output was tested for 180 kΩ load resistance. As shown in Figure 2.8, the five stages are required to reach the output voltage of 9.6V at 0 dBm and a maximum of 33.9V at 20 dBm. The proposed design can power low-power devices instead of batteries by comparing it to prior studies on various voltage multiplier stages of RFEH systems. Low-power systems have been actively investigated to use energy-on-demand from RF-energy harvesting; however, the tiny amounts of energy that can be extracted from RF signals provide an imposing obstacle. In contrast to using electric batteries, this paper effectively generated a significant amount of power with the largest voltage gain [28]. Figure 2.7 shows a single-stage voltage multiplier at 950 MHz utilizing the ADS and HSMS-2850 diode. Figure 2.8. represent the RF harvesting circuit design using 5-stage voltage multipliers with diode HSMS-2850 [7].

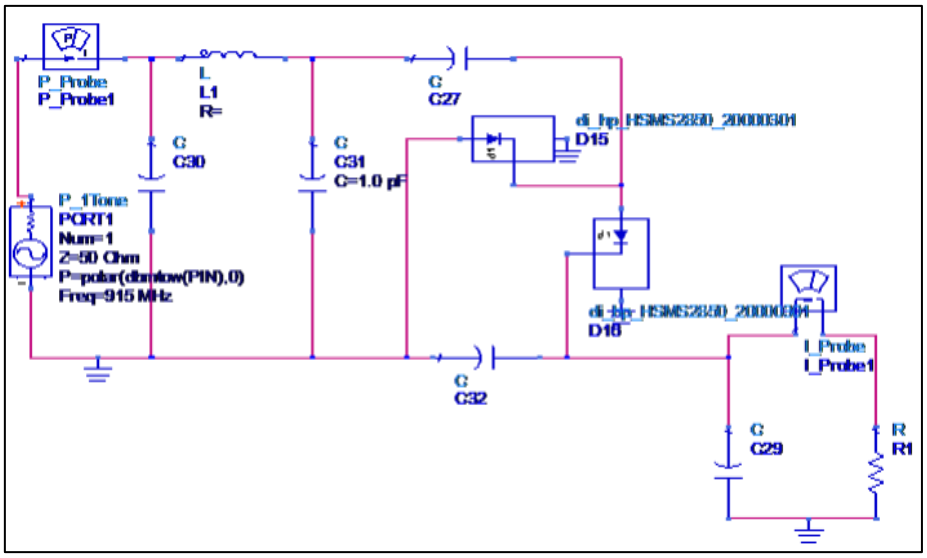


Figure 2. 7. Use the HSMS-2850 diode to create a single-stage voltage multiplier for the 915 MHz ADS program. [7].

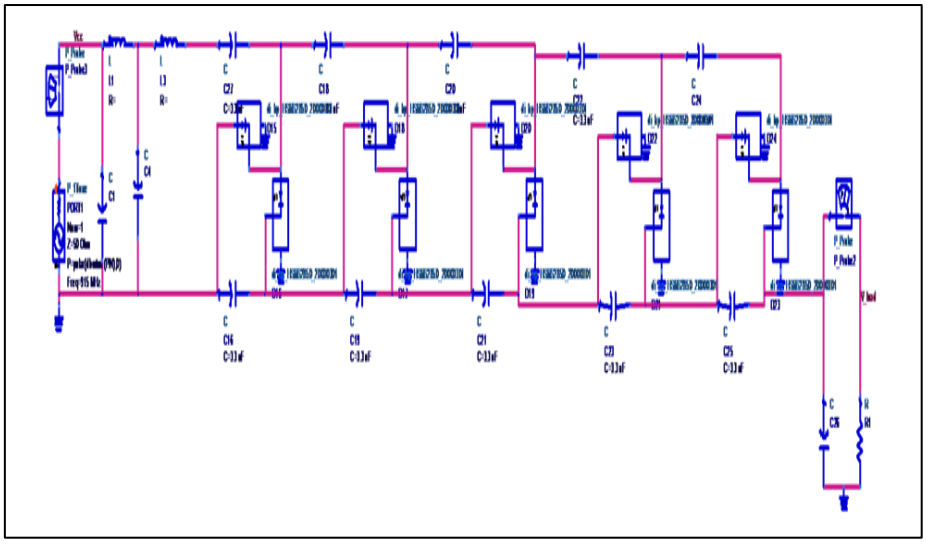


Figure 2. 8. Harvesting circuit design with 5-stage voltage multiplier using diode HSMS-2850 [7].

Ekkaphol Khansalee., et al., in 2015, presented a study of a dual-band energy harvesting system carried out at 2100 MHz and 2450 MHz. The rectifier circuit is designed using a Greinacher voltage multiplexer. Schottky diode HSMS 285C was used as diode. ADS program was used for the designs. The design was carried out at 1.6 kΩ load resistance - 40 dBm and 10 dBm input power. The designed system provides 1.9 V output power at 2100 MHz at 10 dBm input power, 1.245 mA load current, and 24% maximum efficiency, while 1.7 V output power at 2450 MHz at 10

dBm input power, 1.081 mA load current, and 18% maximum efficiency. Figure 2.9 shows the ADS simulation representation of the dual-band rectifier circuit operating at 2100 MHz and 2450 MHz frequencies [29].

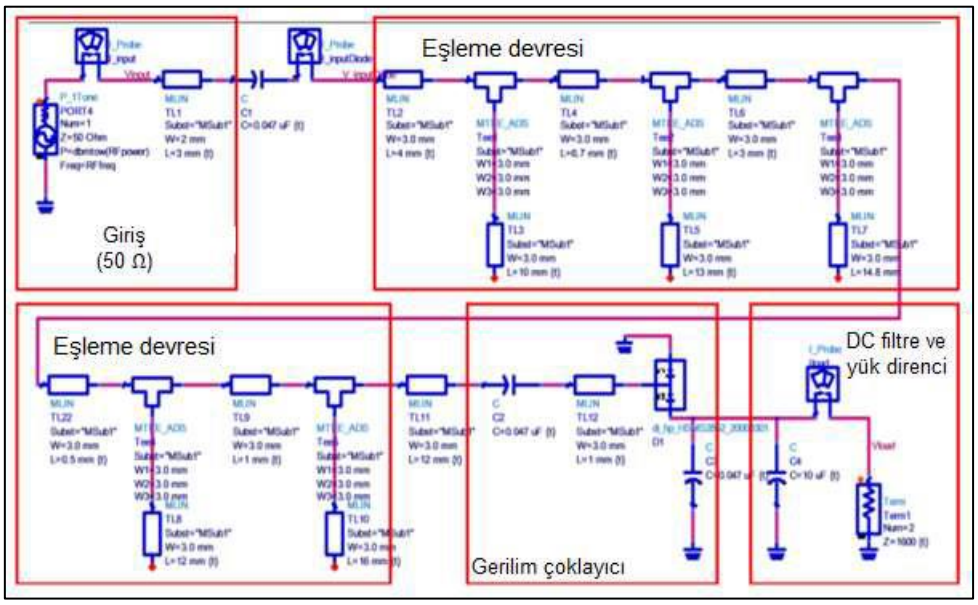


Figure 2.9. Dual-band rectifier circuit simulated by ADS [29].

Rathdharshagorn Suriyakul Na Ayudhya, in 2014, presented in his article a switched-capacitor charge pump circuit with a power scale of more than 10W and voltage exceeding 100V is shown. It swaps out the Dickson's digital switches to produce the desired power for full-bridge power "MosFets" switches. According to experimental findings, voltage conversion, and regulation efficiency are 44.5% and 21.3%, respectively. It was suggested and tried to utilize MOSFET power switches rather than digital switches to boost the output of Dickson charge pumps. Experimental facts support theoretical predictions. For Iout = 0.1A. The efficiency of a high-power DVM circuit using full-bridge MosFet switches is 44.5%. The circuit has a 21.3% voltage regulation [23].

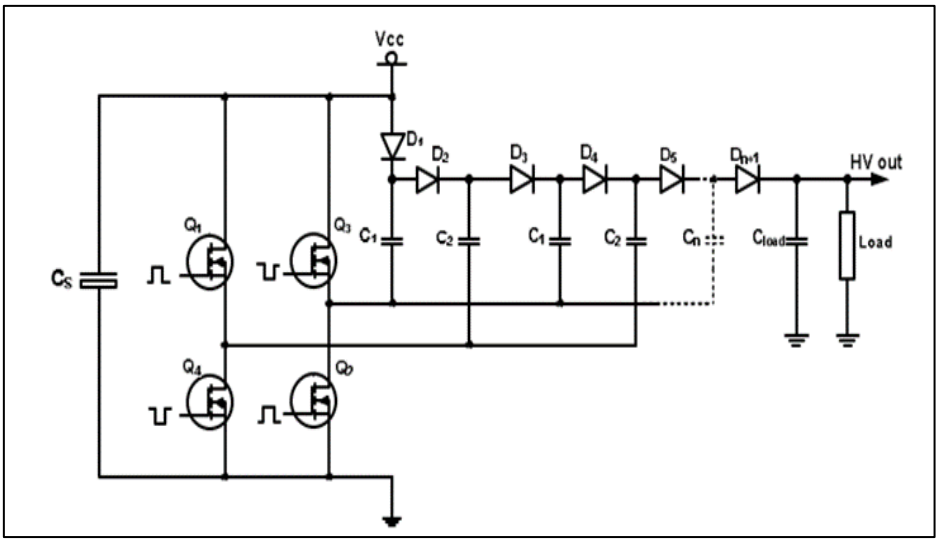


Figure 2.10. High-voltage of DVM design [23].

A theoretical and practical comparison of the Dickson method and the cascade of voltage doublers, two charge pump topologies frequently employed in CMOS integrated circuits, is presented by Baderna, D. et al. in 2006. The comparison uses power efficiency as the primary factor to be considered. In 0.18 mm triple-well CMOS technology, two charge pumps were integrated to compare the topologies. The design of the two charge pumps used the same working clock frequency, store capacitance per stage, and the total number of stages, as shown in Figure 2.11. The comparison between the theoretical and actual results revealed that the voltage doubler system had a greater power efficiency (roughly 13% at Iout 1/4 1 mA), primarily due to the smaller parasitic capacitance [30].

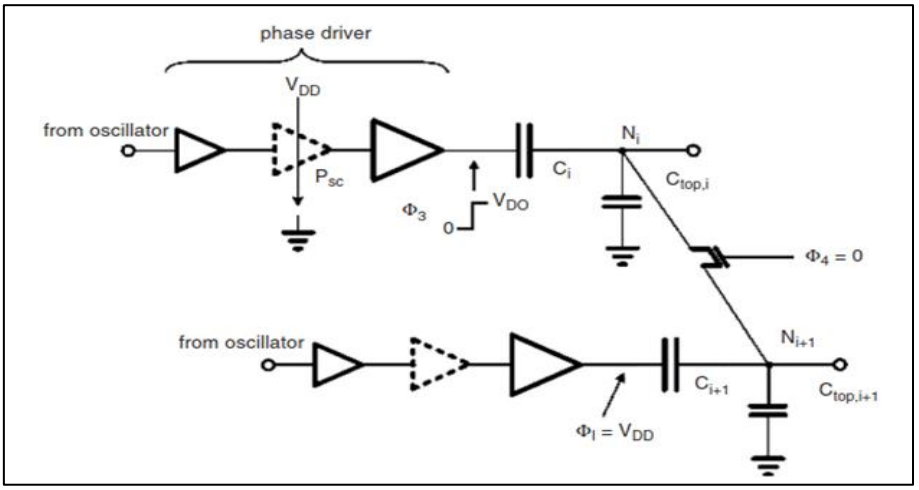


Figure 2.11. The voltage-divider schematically at node Ni [30].

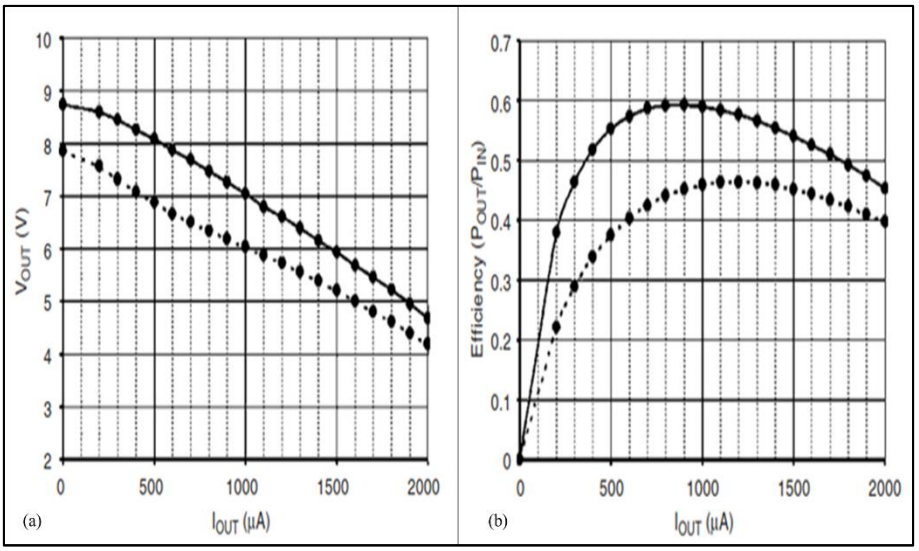


Figure 2.12. The Vout and Efficiency of Dickson charge pump [30].

Figure 12(a). Voltage doubler (solid line) and DVM charge pump (dashed line) measured output characteristics. Figure 12(b). voltage doubler (solid line) and Dickson charge pump (dashed line) efficiency measurements.

Figure 12(a). The estimated values of 1.92 and 2.18 kΩ, respectively, should be compared to the measured output resistance of 1.87 kΩ for the Dickson pump and 2.14 kΩ for the cascade of voltage doublers. Figure 12(b) shows two pumps. As previously stated, the voltage doubler exhibits superior efficiency for any value of Iout because its dynamic losses are lower than those of a Dickson pump, about "2950 and 4800 mW", respectively.

Another vital aspect of RFEH is the design of antennas and impedance-matching circuits. Researchers have investigated different antenna types, such as dipoles, loops, and patch antennas, to optimize the energy transfer between the RF source and the energy harvester. Additionally, impedance-matching circuits have improved energy transfer efficiency and reduced reflections [6,31].

Overall, RFEH in the 915 MHz band has the potential to provide a reliable and efficient source of energy for a wide range of wireless sensor and IoT applications. However, further research is needed to address the technical and regulatory challenges and to develop more efficient and compact energy harvesting solutions [6,17,31].

PART 3

DESIGN OF ENERGY HARVESTING CIRCUIT

A voltage multiplier circuit, also known as a rectifier, is a device used to convert alternating current (AC) to direct current (DC) by multiplying the input signal's voltage. This is useful in various applications, including radio frequency (RF) energy harvesting, where the circuit converts the weak, high-frequency signals from RF sources into usable DC power [9,11].

The basic principle of a voltage multiplier circuit is to take a single AC waveform and convert it into multiple DC output voltage levels by using a series of diodes and capacitors. The diodes are used to rectify the AC waveform and convert it into a pulsating DC signal, while the capacitors are used to smooth out the pulsations and provide a steady DC output [11,32].

There are several types of voltage multiplier circuits, each with unique characteristics and advantages. One of the most common types is the diode-capacitor voltage multiplier, also known as a "charge pump," which uses a series of diodes and capacitors to generate a high DC voltage from a lower AC input. Another popular type is the diode-resistor voltage multiplier, which combines diodes and resistors to generate a lower DC voltage from a higher AC input [11].

One of the main advantages of voltage multiplier circuits is their ability to produce high DC voltage outputs from low AC inputs. This makes them ideal for RFEH applications, where the input signals are typically weak and high-frequency [7]. In these applications, the circuit can be used to convert the weak RF signals into usable DC power, which can then be stored in a battery or used to power other electronic devices [33,34].

Another advantage of voltage multiplier circuits is their high efficiency and low cost. Since they do not require moving parts or complex mechanical components, they can be manufactured relatively cheaply and have a long lifespan. Additionally, they are highly reliable, making them ideal for use in remote or harsh environments [13,32].

In conclusion, voltage multiplier circuits, or rectifiers, are essential to RF-energy harvesting. They convert weak and high-frequency signals into usable DC power. They come in different types, such as diode-capacitor voltage multipliers and diode-resistor voltage multipliers, each with its characteristics and advantages. They are efficient, low-cost, and reliable, making them suitable for remote or harsh environments [35].

This thesis chapter will cover the whole design, starting with the choice of load resistance. Next, we'll discuss the Dickson voltage multiplier and why we chose to utilize it in our design. Besides, some factors to take into consideration while using diodes. The impedance matching mechanism will be applied to the DVM designs in different stages to test the actinolite with and without using it. Also, a comparison result will be made between the matching type through the rectifier circuit. Hence, the quality factor while implementing and testing all the DVM designs using different stages and diodes is suggested in this thesis.

3.1. DIODE SELECTION

When selecting a diode for use in RFEH at 915 MHz, it is essential to consider the following factors:

- Reverse breakdown voltage: The reverse breakdown voltage (V_{br}) is the maximum voltage that can be applied to the diode in the reverse direction before it becomes damaged. The reverse breakdown voltage should be higher than the maximum voltage that will be present in the circuit to ensure the diode is not damaged [1,36,37].
- Forward voltage drops: The forward voltage drops (V_f) is the voltage drop across the diode when it conducts in the forward direction. A low forward

voltage drop minimizes power loss and increases the efficiency of the energy harvesting circuit. The forward voltage drop can be calculated using the Shockley diode as shown in equation 3.1 below [1,38].

$$I = I0(exp(eVf/nkT) - 1) \quad (3.1)$$

- Frequency response: The diode's frequency response is characterized by its capacitance (C_d) and inductance (C_d), affecting the circuit's performance at high frequencies [38,39]. Low capacitance and inductance ensure optimal performance at 915MHz. The capacitance of the diode can be calculated using the equation 3.2 below:

$$C_d = C_j + C_{j0}(1 - \frac{V}{V_j}) \quad (3.2)$$

- Power handling-capability: is determined by its maximum power dissipation (P_d) and maximum forward current (I_f) of the diode. A high-power handling capability ensures the diode can handle the high-power levels in RFEH applications.
- Temperature range: The diode's operating temperature range is determined by its maximum operating temperature (T_{max}) and minimum operating temperature (T_{min}). A wide operating temperature range ensures reliable operation in various environments [10,20].
- Size and cost: The size and cost of the diode should be considered concerning the overall design constraints of the system. A small, cost-effective diode is preferable for RFEH applications [10,40].

Schottky diode is suitable for RFEH at 915MHz because of its low forward voltage drop, high-frequency response, and high-power handling capability. They also have low capacitance and inductance, making them suitable for high-frequency applications.

Based on the above considerations, a Schottky diode is a good choice for RFEH at 915MHz because of its low forward voltage drop, high-frequency response, and high-power handling capability [3,34,41].

A diode and rectifier are often used in RFEH systems to convert alternating current (AC) to direct current (DC). The diode is a semiconductor device that allows current to flow in only one direction, and the rectifier is a circuit that uses diodes to convert AC to DC. The rectifier circuit can be either a half-wave or full-wave rectifier [42].

A half-wave rectifier circuit consists of a single diode and a load resistor. During the positive half of the input AC wave, the diode is forward-biased and conducts current, allowing it to pass through the load resistor and be converted to DC [1, 14]. During the negative half of the input wave, the diode is reverse-biased and does not conduct, blocking the current and preventing it from passing through the load resistor [9,42]. The output of a half-wave rectifier circuit is a pulsating DC wave with the same frequency as the input AC wave but with only half the amplitude. The equation to calculate the DC output voltage is defined in (3.3) below [1,17,32]:

$$V_{dc} = V_m \times (1 + \text{ripple factor}) \times (D) \quad (3.3)$$

Where V_m: the peak value of the AC input voltage, D: the duty cycle and ripple factor measure the ripple present on the output waveform. A full-wave rectifier circuit comprises two diodes and a load resistor [1]. During the positive half of the input AC wave, one diode is forward-biased and conducts current, allowing it to pass through the load resistor and be converted to DC [9]. The other diode is forward-biased during the negative half of the input wave. It conducts current in the opposite direction, allowing it to pass through the load resistor and be converted to DC [20,43]. The output of a full-wave rectifier circuit is a steady DC wave with the same frequency as the input AC wave but with a lower amplitude. The equation to calculate the DC output voltage is defined in equation 3.4 below:

$$V_{dc} = V_m \times (1 + ripple\ factor) \times \left(\frac{2}{\pi}\right) \quad (3.4)$$

Where V_m : the peak value of the AC input voltage, ripple factor measures the ripple present on the output waveform. In RFEH systems, a full-wave rectifier is often preferred because it provides a steady DC output with less ripple and higher efficiency than a half-wave rectifier. It also provides a better input energy utilization than a half-wave rectifier [1,20].

3.2. TPYE OF RFEH DIODES

Several types of Schottky/diodes are commonly used for RF-energy harvesting:

a. Schottky Barrier Diodes (SBD): These diodes have a metal-semiconductor junction, which results in a low forward voltage drop, high-frequency response, and high-power handling capability. They are often used in RFEH applications because of their fast-switching speeds, low noise, and low capacitance.
b. Schottky Tunnel Diodes (STD): These diodes have a P-N-I-N structure, which results in a negative resistance region. They are often used in RFEH applications because of their high-frequency response and fast switching speeds.
c. Schottky Metal-Insulator-Semiconductor (MIS) Diodes: These diodes have a metal-insulator-semiconductor structure, resulting in a low capacitance and high-frequency response. They are often used in RFEH applications because of their high-frequency response and fast switching speeds.
d. Schottky Metal-Oxide-Semiconductor (MOS) Diodes: These diodes have a metal-oxide-semiconductor structure, resulting in a low capacitance and high-frequency response. They are often used in RFEH applications because of their high-frequency response and fast switching speeds.
e. Schottky Silicon-Carbide (SiC) Diodes: These diodes are made of Silicon Carbide material, resulting in high breakdown voltage and high-temperature operation. They are often used in RFEH applications because of their high-frequency response, fast switching speeds, and high-temperature operation capability.

It's worth noting that the selection of the appropriate Schottky diode type depends on the specific requirements of the RFEH system, such as power handling capability, frequency response, and temperature range, as well as the cost and size constraints of the overall design.

In this thesis (HSMS-2822, HSMS-2852, and HSMS-2862), diodes are selected for application in the rectifier for the RFEH system for 915 MHz. In addition, the diodes are designed for RFEH in wireless power transfer systems that can operate at 915 MHz. They both convert the RF signal received by the antenna into a DC voltage that can be used to power a device.

Besides, the HSMS-2822, HSMS-2852, and HSMS-2862 are high-speed Schottky diodes that can be used in a DVM for RFEH at 915 MHz. The DVM is a popular circuit topology for RF-energy harvesting, capable of generating a high output voltage from a low input voltage by stacking a series of diode-capacitor stages. However, using these diodes in the DVM for RFEH can present different challenges and problems [17,25,44].

Moreover, the HSMS-2822, HSMS-2852, and HSMS-2862 diodes have different forward voltage drops, affecting their performance in the Dickson voltage multiplier. The HSMS-2822 has a low forward voltage drop of 0.39V, making it suitable for use in the low voltage range of the Dickson voltage multiplier. The HSMS-2852 has a slightly higher forward voltage drop of 0.46V, making it better suited for use in the higher voltage range of the multiplier. The HSMS-2862 has the highest forward voltage drop of 0.58V, making it suitable for use in the highest voltage range of the multiplier [10,17,25].

One problem that can arise when using these diodes in the Dickson voltage multiplier is the potential for voltage breakdown. As the voltage increases across each stage of the multiplier, the voltage across each diode also increases, potentially leading to breakdown if the diode's reverse voltage rating is exceeded. This can be mitigated by choosing a diode with a higher reverse voltage rating or limiting the voltage across each diode through careful design [27].

Another challenge that can arise when using these diodes in the Dickson voltage multiplier is the potential for parasitic capacitances and inductances to affect the circuit's performance [45]. The high frequency of the RF signal at 915 MHz can cause parasitic capacitances and inductances to become more significant, leading to reduced efficiency and output voltage. This can be addressed through careful layout and component selection, including using low-inductance capacitors and high-frequency decoupling [46].

The $\mathrm{HSMS-2822, HSMS-2852, and\ HSMS-2862}$ can be used in the Dickson voltage multiplier for RFEH at 915 MHz. However, careful consideration must be given to the diode's forward voltage drop, reverse voltage rating, and the potential for parasitic capacitances and inductances. By addressing these challenges through careful design and component selection, the efficiency and output voltage of the circuit can be maximized.

3.4. THEORY OF MATCHING NETWORK TOPOLOGY

The design of $\mathrm{LC, LL, T,}$ and PI matching impedance networks is an essential concept in electrical engineering, particularly in the design of radio frequency (RF) circuits [10,42]. The goal of impedance matching is to optimize the energy transfer between a circuit and a load or source by ensuring that the impedances at the input and output of the system are equal. This can be achieved using $\mathrm{LC, LL, and}$ PI matching networks [37]. An LC matching network is a type of circuit that uses a combination of inductors (L) and capacitors (C) to transform the impedance of a circuit. The circuit is designed so that the inductors and capacitors are connected in such a way that they cancel out the reactance of the load or source impedance. This results in a matched impedance, allowing maximum energy transfer between the circuit and the load or source [37,40].

An LL matching network is a type of circuit that uses a combination of two inductors (L) to transform the impedance of a circuit. The circuit is designed to connect the two inductors in series with the load impedance and in parallel with the source impedance. The goal is to cancel out the reactance of the load or source impedance, resulting in a

matched impedance, allowing maximum energy transfer between the circuit and the load or source [25,37].

The most common type of LC matching network is the pi network. The pi network comprises two inductors and two capacitors arranged in the Greek letter pi (π) shape. The circuit's input impedance is connected to one side of the network, and the load or source impedance is connected to the other. The two inductors are connected in series between the input and output, and the two capacitors are connected in parallel between the input and output [10,17]. The design of an LC, LL, and PI matching network begins with calculating the complex impedance of the load or source. This can be done using the following equation 3.5 below:

$$Z = R + Jx \tag{3.5}$$

Where Z is the complex impedance, R is the resistance, and X is the reactance. The goal of the LC, LL, and PI matching/network is to-cancel out the reactance of the load or source impedance. Once the complex impedance of the load or source has been calculated. The values of the inductors and capacitors have been determined using the following mathematical equations 3.6, 3.7, and 3.8 below:

- For LC matching;

$$L = \frac{Xl}{2\pi f} \tag{3.6}$$

$$C = \frac{1}{(2\pi f Xc)} \tag{3.7}$$

- For LL matching;

$$L1 = L2 = \frac{(Xl + Zl)}{2\pi f} \tag{3.8}$$

Where; "L": is the inductance,"C" is the capacitance, f is the frequency of operation, X_l is the desired inductive reactance, X_c is the desired capacitive reactance, Z_l is the load impedance, and L1 and L2 are the values of the two inductors [47].

The above-described equations are used to design the LC, LL, and PI matching networks. Each network has its advantages based on the specific requirements of the circuit and the load or source impedance [48].

In summary, the design of LC, LL, and PI matching impedance networks is an essential concept in the field of electrical engineering, and it is used to optimize the transfer of energy from one circuit to another. LC and LL matching networks use a combination of inductors and capacitors (LC) or inductors (LL) to cancel out the load's or source impedance's reactance, resulting in a matched impedance. The PI matching network is a particular case of an LC matching network [10,17,25].

3.5. THE QUALITY/FACTOR OF THE MATCHING IMPEDANCE

Improving the quality factor, or Q-factor, of LC, LL, and PI matching impedances in RFEH is essential in electrical engineering. The Q-factor measures the circuit's ability to transfer energy from the main source to the load efficiently, and a high Q-factor indicates a more efficient circuit [13,17]. There are various methods to improve the Q-factor of LC, LL, and PI matching impedances, and one of these methods is using mathematical equations [17].

In addition to the resonant circuits, there are other methods to improve the Q-factor of LC, LL, and PI matching impedances. One approach is to use a transformer. Transformers can be used to match the impedance of the source to the load, improving energy transfer efficiency. Another method is to use a matching network, such as pi or T-network, which can be designed to match the impedance of the source to the load as below in equation 3.9 [17,25,49]:

$$Q = \pi \frac{maximum\ amount\ of\ energ}{energy\ losses\ per\ cycle} \tag{3.9}$$

In the case of LC matching impedance, the Q-factor can be improved by using a parallel resonant circuit. A parallel resonant circuit is an LC circuit in which the inductor and capacitor are connected in parallel. The Q-factor of a parallel resonant circuit can be calculated using the following equation:

$$Q = \frac{(Xl - Xc)}{R\ (Xl + Xc)} \tag{3.10}$$

Where; Q is the Q-factor, R is the resistance, Xl is the inductive reactance, and Xc is the capacitive reactance. By adjusting the values of the inductor and capacitor, the Q-factor can be optimized to achieve maximum energy transfer efficiency.

In the case of LL matching impedance, the Q-factor can be improved by using a series resonant circuit. A series resonant circuit is an LC circuit in which the two inductors are connected in series with the load impedance and in parallel with the source impedance. The Q-factor of a series resonant circuit can be calculated using the following equation:

$$Q\ = \frac{(Xl * Xc)}{R\ \ (Xl + Xc)} \tag{3.11}$$

Where; Q is the Q-factor, R is the resistance, Xl is the inductive reactance, and Xc is the capacitive reactance. By adjusting the values of the two inductors, the Q-factor can be optimized to achieve maximum energy transfer efficiency. For π matching impedance, the Q-factor is calculated by the same equation as the LC matching impedance. The π matching impedance is a particular case of LC matching impedance, and the same equation can be used to calculate the Q-factor [17,35].

In summary, improving the Q-factor of a matching impedance in RFEH can be achieved through several methods, including mathematical equations. Using parallel or series resonant circuits, transformers, and matching networks can improve the Q-factor of a matching impedance and increase energy transfer efficiency. The Q-factor is calculated using the equations above. Selecting the selected types of matching impedance networks for the 900Hz of the RF-energy harvesting will be helpful.

3.5. IMPROVE EFFICIENCY IN RF-ENERGY HARVESTING

Increasing the effectiveness of RFEH is a critical goal in electrical engineering. There are various methods to improve the efficiency of RF-energy harvesting, and one of

these methods is using mathematical equations [39]. One method to improve the efficiency of RFEH is to use a rectifier circuit. A rectifier circuit converts the alternating current (AC) from the source into direct current (DC) that can be used to charge a battery or power a load. The efficiency of a rectifier circuit can be calculated using the following equation 3.10 below:

$$\text{Efficiency} = \frac{P_{DC}}{P_{AC}} \times 100\% \quad (3.12)$$

PDC is DC's output power, and PAC is the input power of AC. Adjusting the rectifier circuit's design and the efficiency can be increased.

Another method to improve the efficiency of RFEH is to use a matching circuit. A matching circuit matches the impedance of the source to the load, improving energy transfer efficiency. The efficiency of a matching circuit can be calculated using the following equation 3.11 below:

$$\text{Efficiency} = \frac{P_{Load}}{P_{S\text{source}}} \times 100\% \quad (3.13)$$

where Pload is the output power to the load, and Psource is the input power from the source. By adjusting the design of the matching circuit, the efficiency can be increased [37, 51]. In addition to the rectifier and matching circuits, there are other ways to improve the efficiency of RF-energy harvesting. One method is to use a voltage boost converter which increases the voltage of the harvested energy to a level suitable for the load. Another approach is to use a power management circuit, which optimizes the power usage of the harvested energy to minimize power loss [31,46].

In summary, increasing the effectiveness of RFEH can be achieved through several methods, including mathematical equations. The use of rectifier circuits, matching circuits, voltage boost converters, and power management circuits can all improve the efficiency of RF-energy harvesting. The efficiency is calculated by using the equations above, and it will be helpful to to select the best circuit topology to optimize the efficiency of RF-energy harvesting.

3.6. HARVESTING SYSTEM DESIGN AND SIMULATION

By utilizing harmonic balance techniques, the Advanced-develop-System (ADS) was implemented to model a DVM suggested stages and two modalities of a diode. Avago Technologies' three models of Schottky diodes which are; the HSMS-2822, HSMS 2852 , and HSMS-2862 have been simulated in the suggested system as shown in Appendix 1. Besides, numerous impedance matching circuit types, such as L T pi matching networks, will be used to design a multi-stage DVM system from two to six stages, depending on the suggestion system. The results for the planned circuit were obtained using several different load resistance conditions: 25, 50,100, 500,1000, to 2500 KΩ. Regardless of the circumstance, the output voltage rises with growing input power up until the reverse breakdown voltage of the Schottky diodes is surpassed.

The output voltage curves remain largely constant for the remaining power levels. Furthermore, when the number of stages is increased, the maximum DC output voltage rises simultaneously in direct relationship to the value of data and output. Another fact is, Lower rectified output voltages are the result of adding more stages. Hence, it is due to the need for higher input voltages to forward bias the Schottky diodes utilized in further stages, and it is anticipated that using a matching network will increase the output-voltage of the DVM at low power result since the matching network offers a gain. Besides will be further demonstrated in the following chapters.

PART 4

SIMULATION AND RESULT

Among the main factors that directly affect the design of the circuit and its efficiency are the diode used, the circuit impedance, and the load resistance. In this thesis, using the ADS program, different conditions will be applied to circuits designed under several variable conditions. Thus, a comparative study of the results to determine the highest efficiency of the circuit through the data that will be applied.

4.1. THE EFFECTED OF LOAD

The efficiency of the Dickson voltage rectifier, used in radio frequency (RF) energy harvesting, is influenced by the load placed on it. The DVM rectifier is a circuit that converts AC signals into DC signals for energy-harvesting applications. At low load conditions, the efficiency of the DVM rectifier is high because the input power is proportional to the square of the input voltage. However, as the load on the rectifier increases, the efficiency begins to decrease due to power losses in the diode and other components.

For 915 MHz RF-energy harvesting, the load on the Dickson voltage rectifier can significantly impact its overall efficiency. At high load conditions, the rectifier may be unable to provide sufficient power to the load, leading to decreased efficiency. On the other hand, if the load is too low, the rectifier will waste a lot of energy in heat. Choosing the proper load resistance to achieve maximum efficiency of the Dickson voltage rectifier in RF-energy harvesting is essential. This can be determined by optimizing the load resistance based on the input power, voltage, and other relevant parameters.

Moreover, the efficiency of the DVM rectifier in RFEH for 915 MHz depends on the load placed on it.

The efficiency decreases with increasing load but also reduces with too low of a load. Finding the optimal load resistance is vital to achieving maximum efficiency. Besides, using two types of Schottky diodes HSMS 2822 and HSMS 2862 in the designed circuit, different load resistances are applied as follows (25, 50, 100, 500, 1000, and 2000) KΩ with various stage number stages of the DVM, which will be between 2 to 6 stages and the comparison result will be made.

4.2. THE HARVESTING CIRCUIT FOR HSMS 2822 DIODE

In this part, the circuits of DVM will be designed and tested by using HSMS 2822 Diode operating at a frequency of 915 MHz. In this section, the circuits of DVM will design at different stages from 2 to 6 and apply three different matching impedance topologies L, T and π matching networks. Each circuit will be simulated individually to test the Vout and the efficiency. The results will discuss.

4.2.1. The DVM Design With L Matching

A- the design of two stages for DVM

Figures 4.1 and 4.2 below represent the suggested system by using the ADS program to simulate the DVM. Figure 4.1 shows the system using L matching applied to the DVM. Figure 4.2 shows the system without using matching impedance.

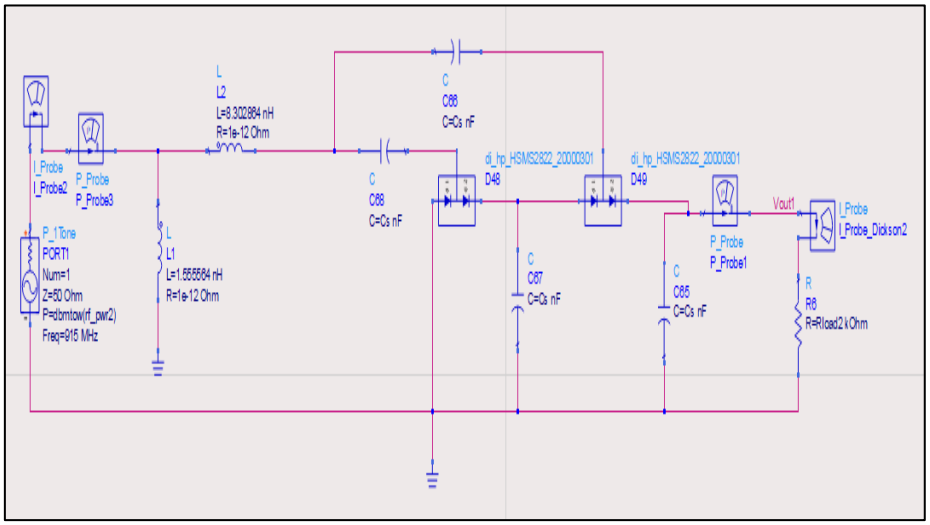


Figure 4.1. The design of two DVM stages with LL-matching impedance.

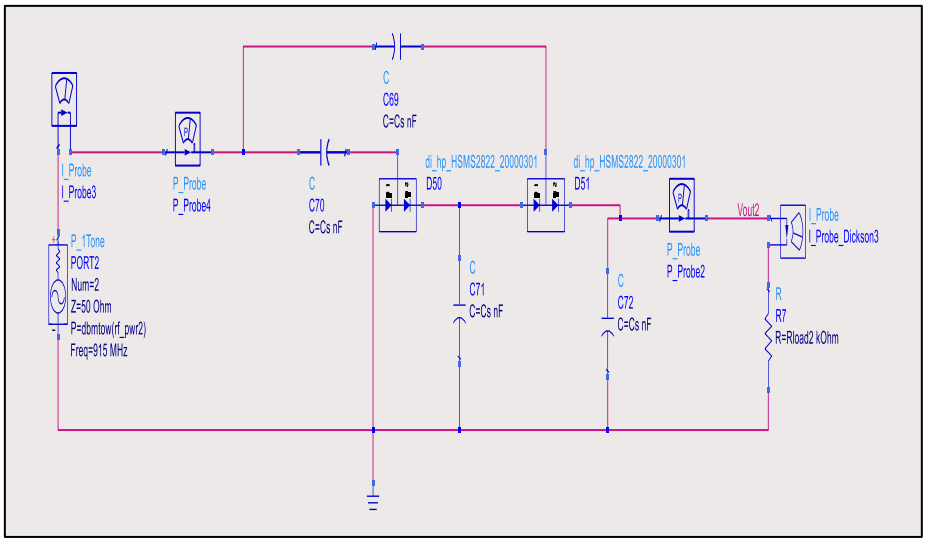
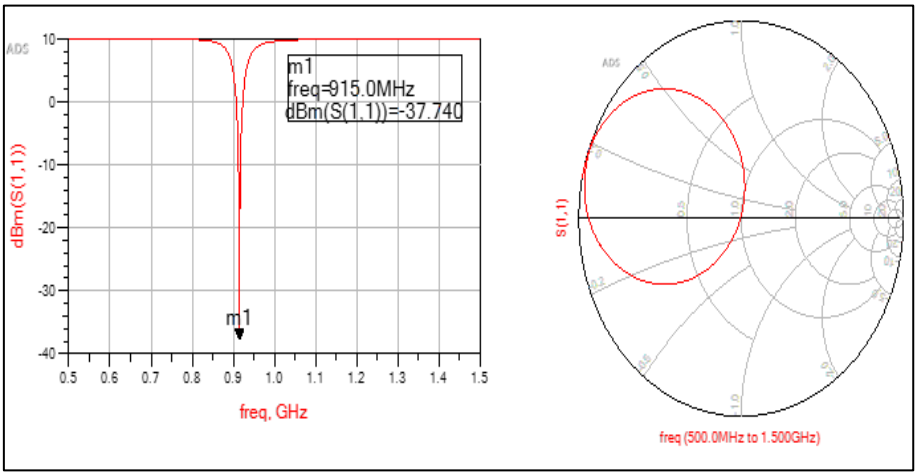
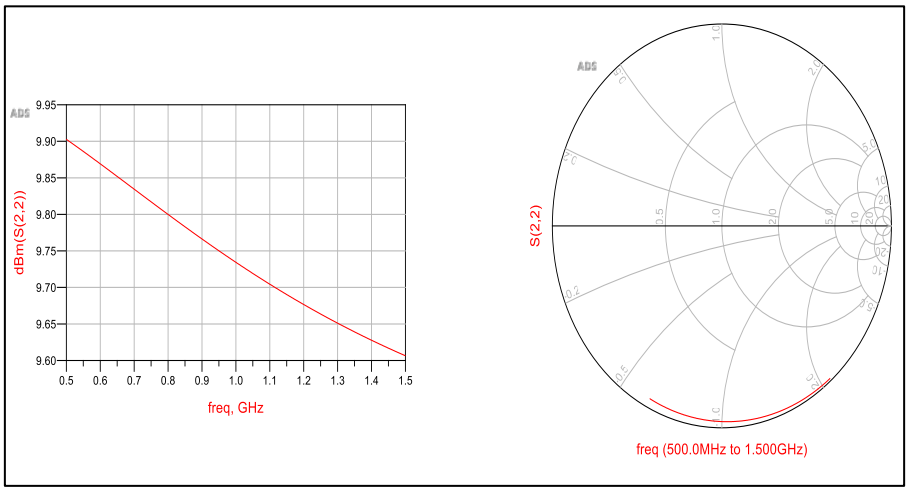


Figure 4.2. The design of two DVM stages without matching impedance



(a) (b)



(c) (d)

Figure 4.3. The $S_{(1,1)}$ for two stages of DVM with and without matching impedance

Figure 4.3(a) shows the $S_{(1,1)}$ for the two stages of DVM using L matching, and the result represents the matching around 37.740 dB. Figure 4.3(b) shows the Smith chart of the matching impedance for 915 MHz applied from 500 MHz to 1500 MHz. Figure 4.3(c) shows the $S_{(1,1)}$ for the two stages of DVM without using the L matching, and the results represent the referral mismatch. Figure 4.3(d) shows the Smith chart without using the matching impedance for 915 MHz that is applied from 500 MHz to 1500 MHz.

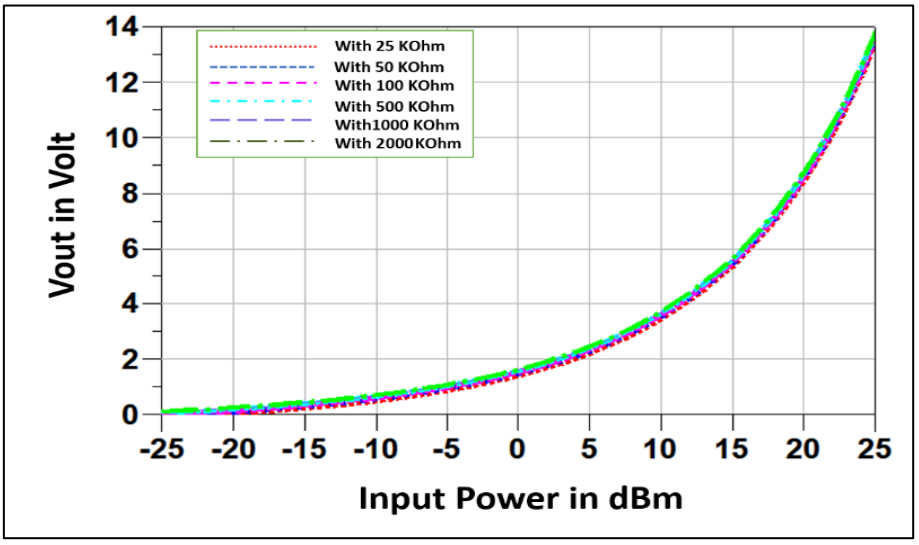


Figure 4.4. The V_{out} of two stage DVM using L matching impedance for HSMS 2822 diode

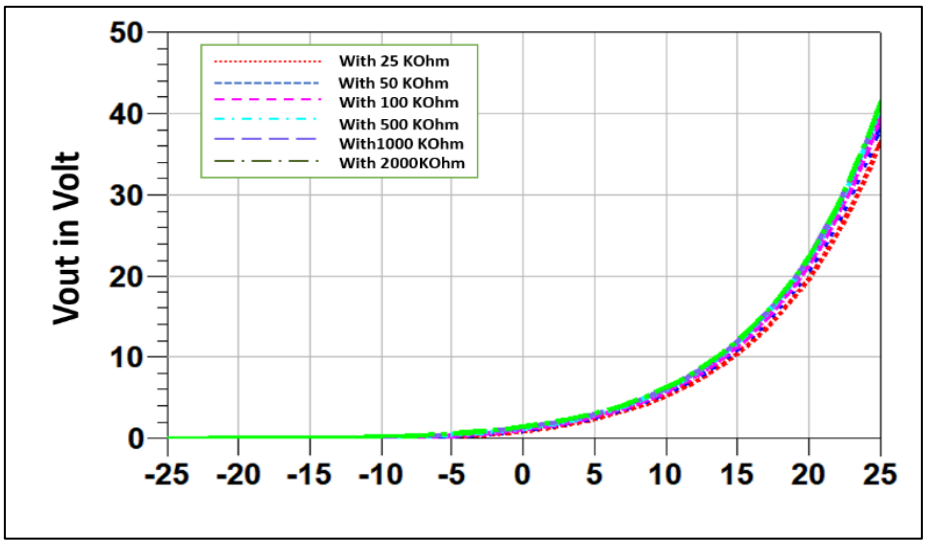


Figure 4.5. The V_{out} of two stage DVM without matching impedance for HSMS 2822 diode

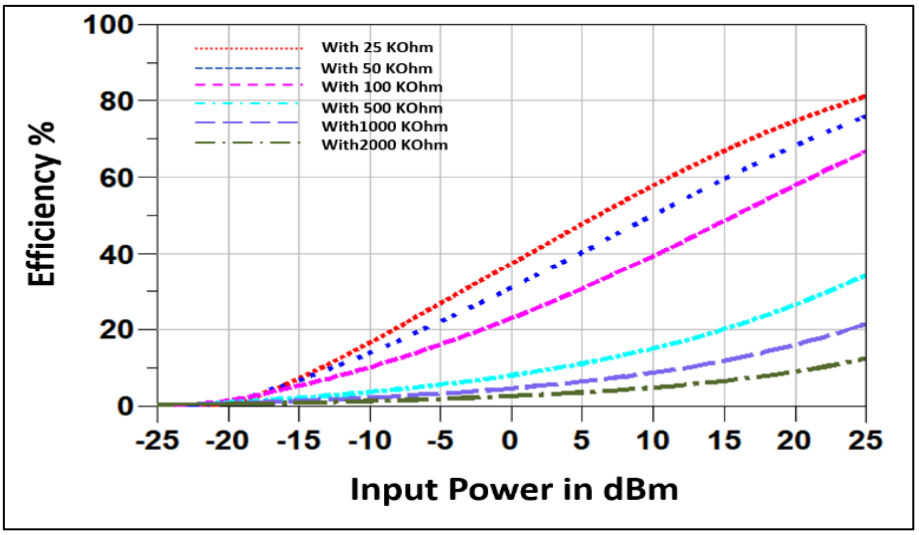


Figure 4.6. The efficiency of two-stage DVM using L matching impedance for HSMS 2822 diode

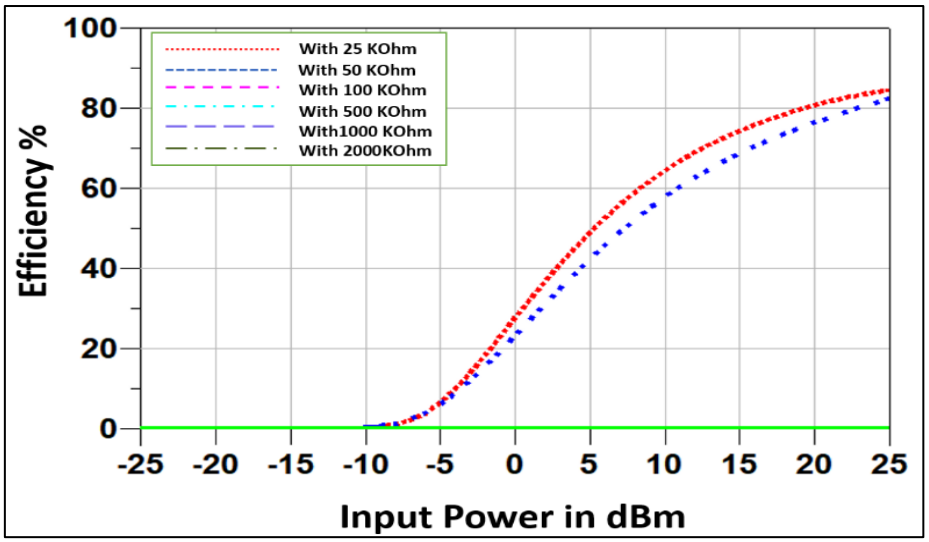


Figure 4.7. The efficiency of two-stage DVM without matching impedance for HSMS 2822 diode

Figure 4.4 represents the Vout by applying the L matching, and the result shows that the period (-25 to 25) dBm of input power starts from -20 dBm, about 0.735V for all the load conditions. Besides, the value of the Vout has reached 14V without problems. Figure 4.5 represents the Vout of the system without using the matching impedance, and the result of the V out, as shown for the same period, started from -5 dBm to reach 40V inaccurately. Figure 4.6 and figure 4.7 represents the efficiency of the circuit with and without using the matching impedance, and the result shows the effect of the

matching network in the system to make it stable and compatible. The efficiency has been affected by the change of the loads; the 20 KΩ of the load has 80% at 25 dBm in contrast to the higher value resistance, which was the efficiency ratio of 15%. In the case without using L matching, the efficiencies are not stable, which is the high efficiencies that can be seen with 25 and 50 KΩ, and the other lodes are zero.

B-design of three stages for DVM

Figures 4.8 and 4.9 below represent the suggested system by using the ADS program to simulate the DVM. Figure 4.8 shows the three stages of the DVM system using L matching that is applied to the DVM. Figure 4.9 exhibits the system without using matching impedance.

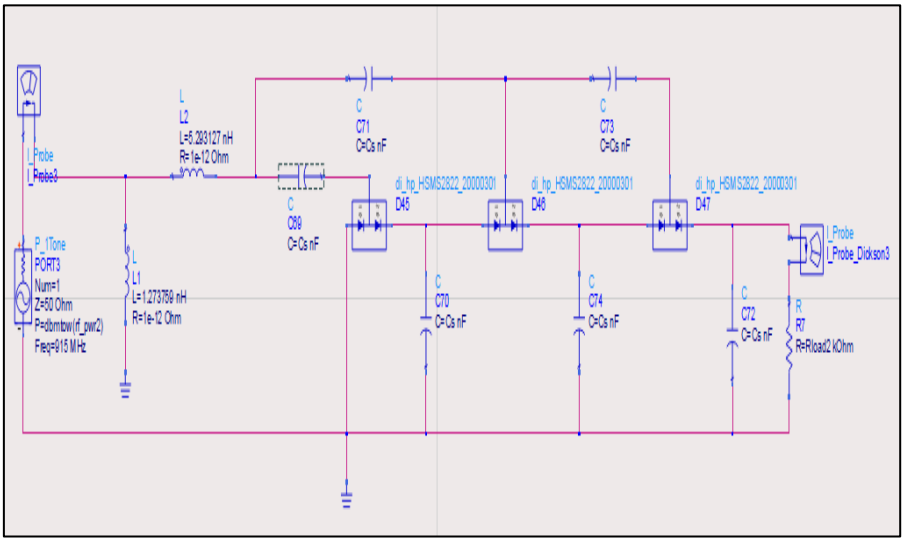


Figure 4. 8. The three stages of DVM with L-matching impedance

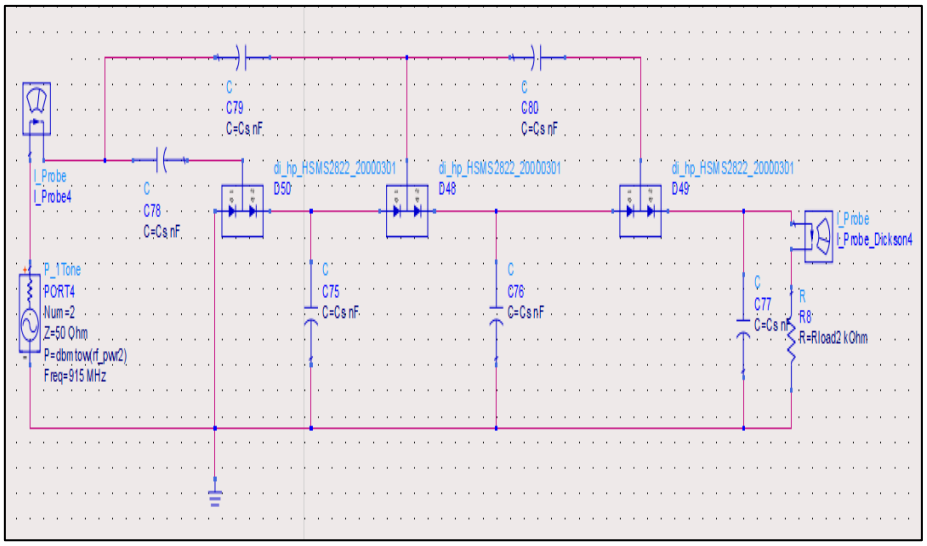
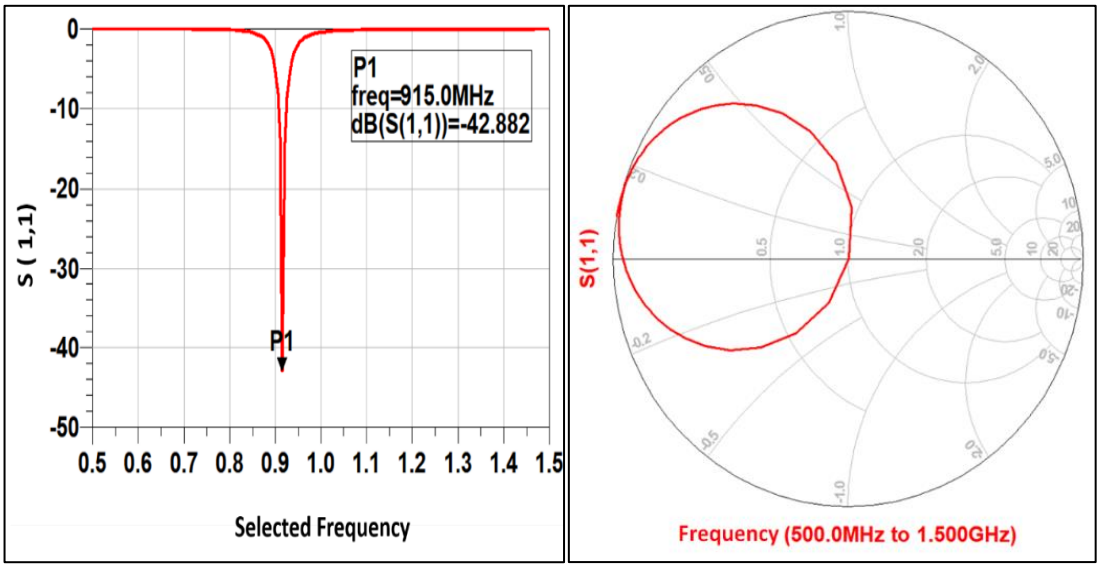


Figure 4. 9. The three stages of DVM without matching impedance



(a) (b)

Figure 4. 10. The $S_{(1,1)}$ for three stages of DVM with and matching impedance

Figure 4.10(a) shows the $S_{(1,1)}$ for the three stages of DVM using L matching, and the result represents the matching around -42.882 dB. Figure 4.10(b) shows the Smith chart of the matching impedance for 915 MHz that applied from 500 to 1500 MHz.

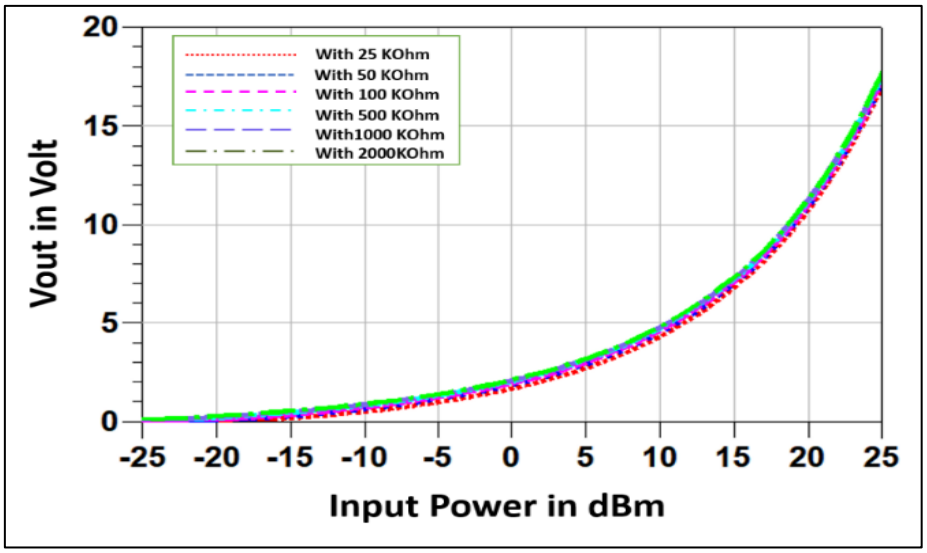


Figure 4.11. The V_{out} of three stages DVM using L matching impedance for HSMS 2822 diode

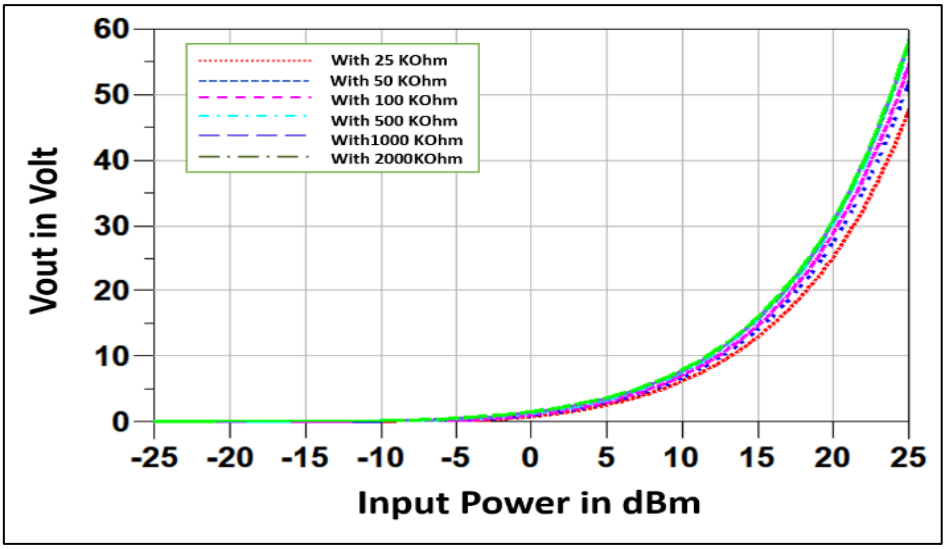


Figure 4.12. The V_{out} of three stages DVM using L matching impedance for HSMS 2822 diode

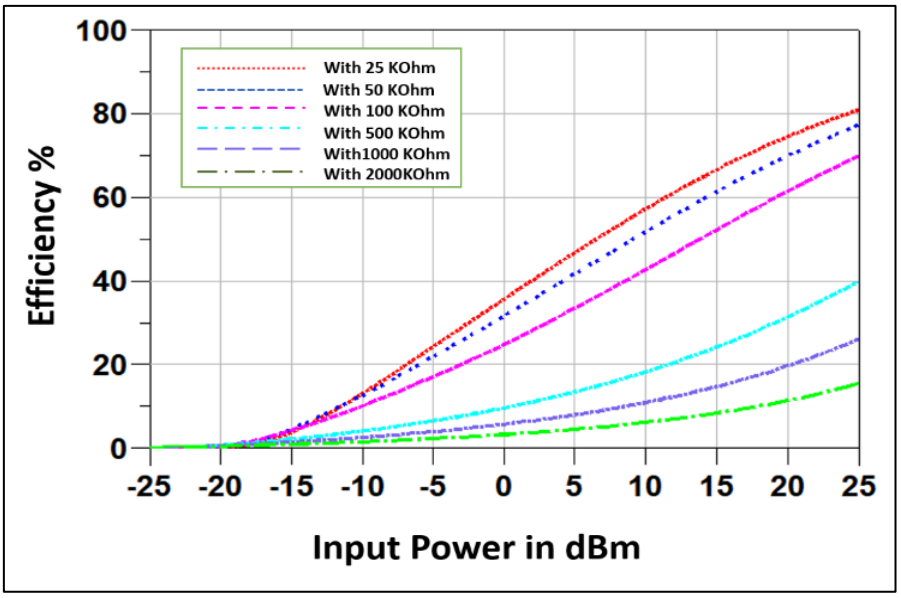


Figure 4.13. The efficiency of three stages DVM using L matching impedance for HSMS 2822 diode

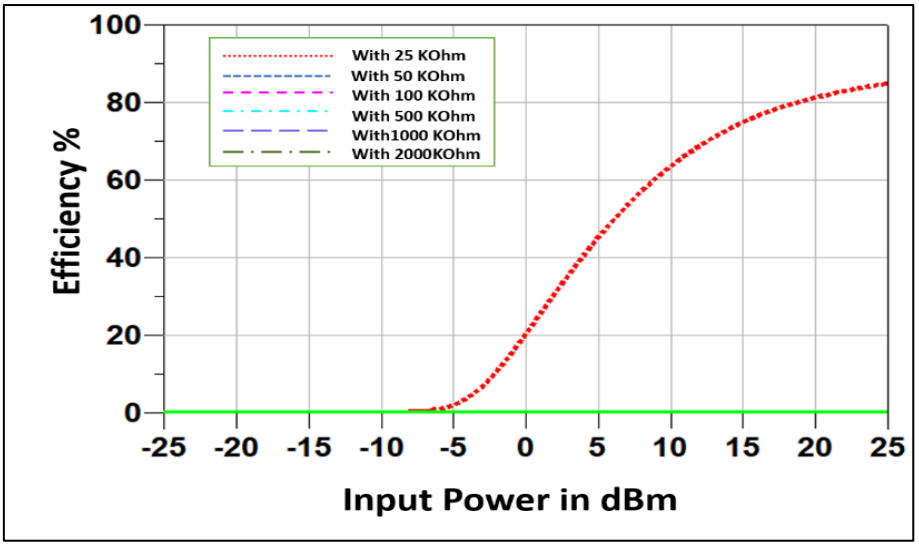


Figure 4.14. The efficiency of three stages DVM without matching impedance for HSMS 2822 diode

Figure 4.11 represents the Vout by applying the L matching for the three stages of DVM, and the result shows that the period (-25 to 25) dBm of input power starts from -15 dBm about 0.326 V for all the load conditions. Besides, the value of the Vout is about 17.3 V at -25 dBm without problems. Figure 4.12 represents the Vout of the system without using the matching impedance, and the Vout result for the same period started from -5 dBm to reach 40V inaccurately at 25 dBm. Figure 4.13 and Figure 4.14

represents the efficiency of the circuit with and without using the matching impedance. The result shows the effect of the matching network in the system to make it stable and compatible with the matching impedance. The efficiency has been affected by the change of the loads at all simulation steps; the 25 KΩ of the load has about 80% at 25 dBm in contrast to the higher value resistance, which was the efficiency ratio of 17.5%. In the case without using L matching, the efficiencies are not stable high efficiencies can be seen with 25 and 50 KΩ, and the other lodes are zero.

C- design of four stages for DVM

Figures 4.15 and 4.16 below represent the suggested system using the ADS program to simulate the four stages of DVM circuits. Figure 4.15 shows the four stages of DVM system by using L matching. Figure 4.16 shows the system without using matching impedance.

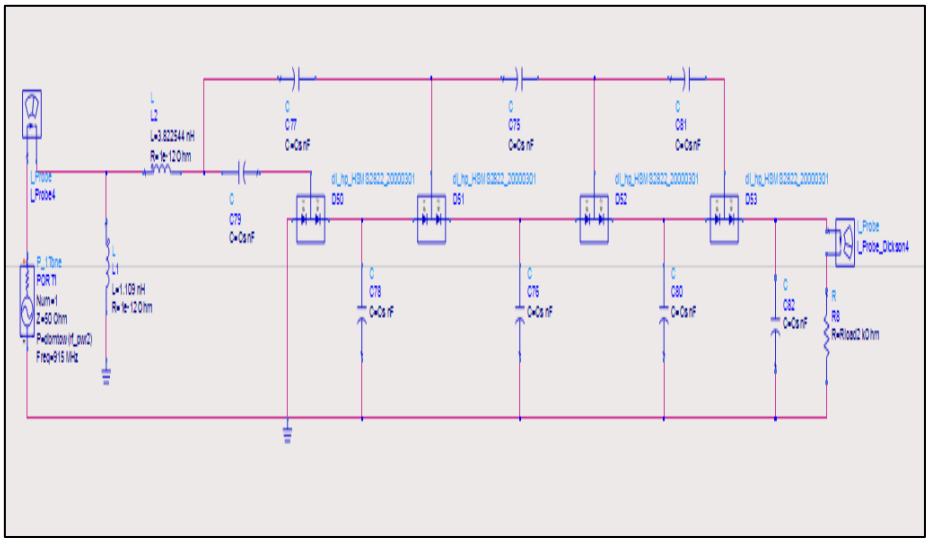


Figure 4. 15. The four stages of DVM with L-matching impedance

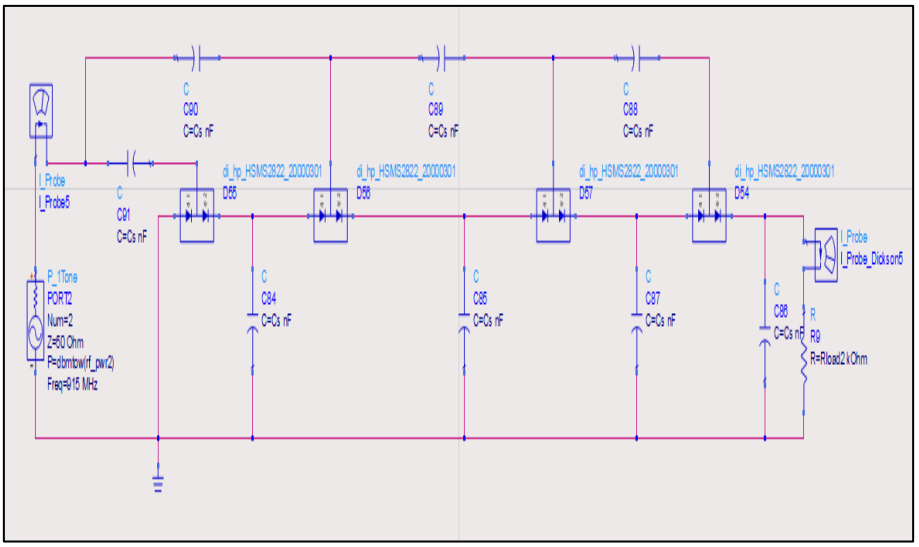
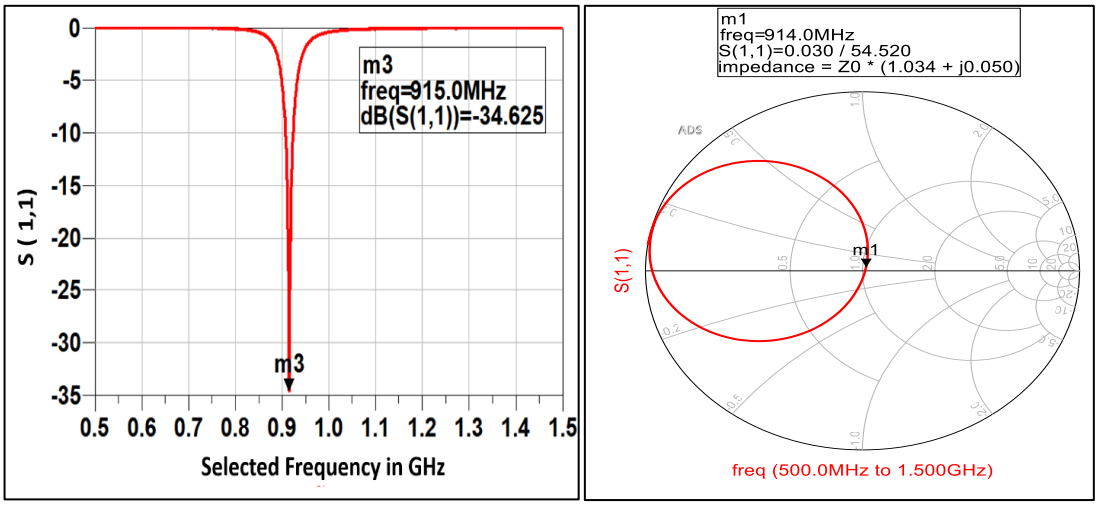


Figure 4. 16. The four stages of DVM without matching impedance



(a) (b)

Figure 4. 17. The $S_{(1,1)}$ for four stages of DVM with matching impedance

Figure 4.17(a). shows the $S_{(1,1)}$ for three stages of DVM with matching impedance and the result of about -37.625 dB. Figure 4.17(b) shows the Smith chart of the matching impedance for 915 MHz that applied from 500 to 1500 MHz.

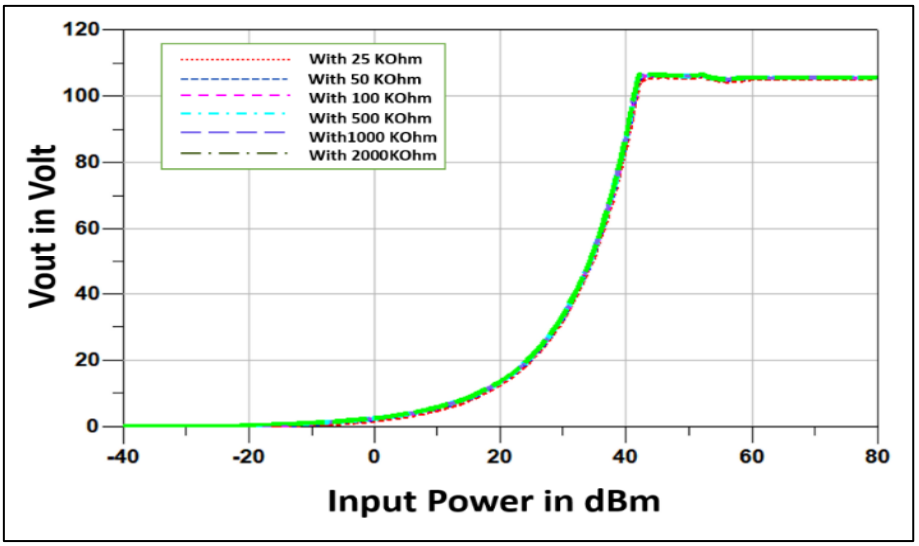


Figure 4. 18. The V_{out} of 4-stages DVM using L matching impedance for HSMS 2822 diode

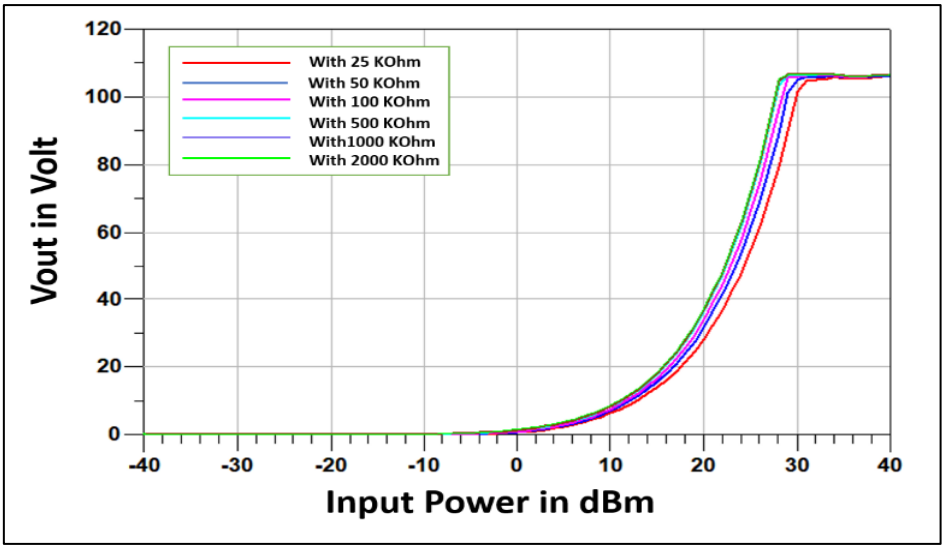


Figure 4. 19. The V_{out} of 4-stages DVM using without matching impedance for HSMS 2822 diode

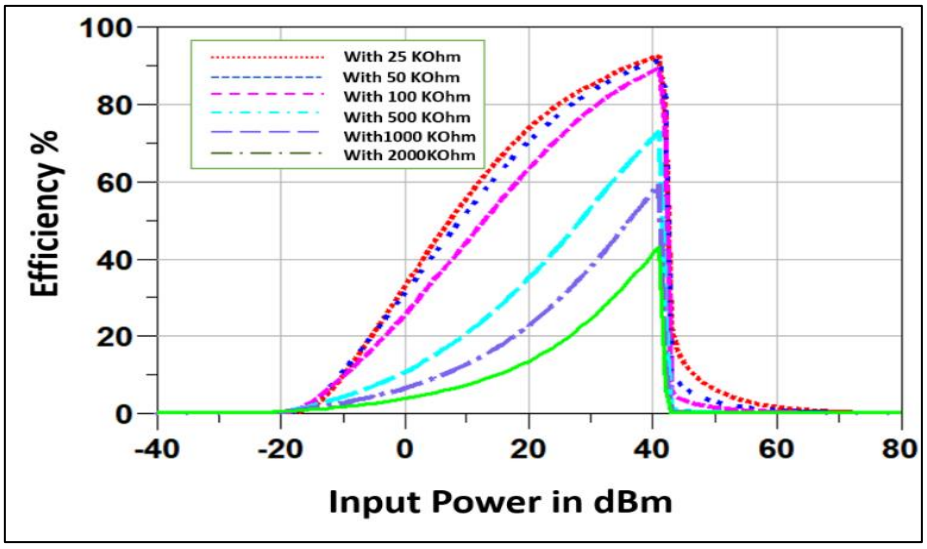


Figure 4. 20. The efficiency of 4-stages DVM using L matching impedance for HSMS 2822 diode.

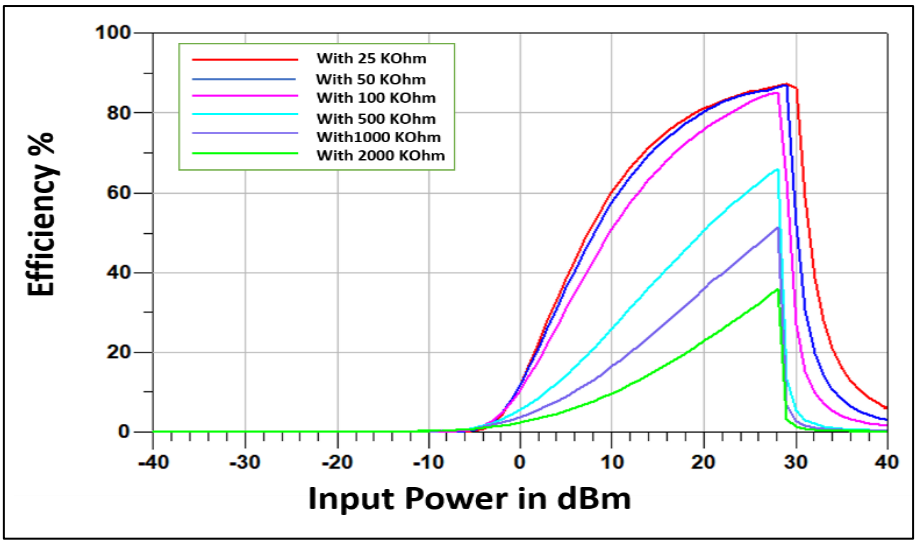


Figure 4. 21. The efficiency of 4-stages DVM without matching impedance for HSMS 2822 diode.

Figure 4.18 shows the value of the output voltages using different load resistors with L matching impedance network for the period from -40 to 80 dBm. The simulation result shows the difference between the values of the voltages with the effect of the almost equal load resistances as the trend starts upward, reaching a value of 25 volts at 20 dBm, and the highest imaginary circuit value that can be achieved, 100 volts at 40 dBm.

Figure 4.19. The value of the output voltages without using the L matching impedance network shows that the outputs of the circuit started from the period -3 dBm, unlike the previous figure, and the output values began to increase, reaching a value of 40 volts in 20 dBm and a value of 100 volts in 30 dBm.

Figure 4.20 shows the efficiency value of the circuit using L-matching impedance. The results show that the efficiency value changes with the change in the load value. The highest efficiency value of the circuit obtained with the lowest weight of the load is 25 KΩ, which reaches 88.5%, and the lowest efficiency value is 42% when the resistance value is 2000 KΩ.

Figure 4.21. It is described as showing the efficiency value of the circuit using L-matching impedance, and the results show that the efficiency value changes with the change in the load value as well, but with less importance than the previous figure.

D- The design of five stages for DVM

Figures 4.22 and 4.23 below represent the suggested system by using the ADS program to simulate the five stages of DVM circuits. Figure 4.22 shows the four stages of the DVM system by using L matching. Figure 4.23 shows the system without using matching impedance.

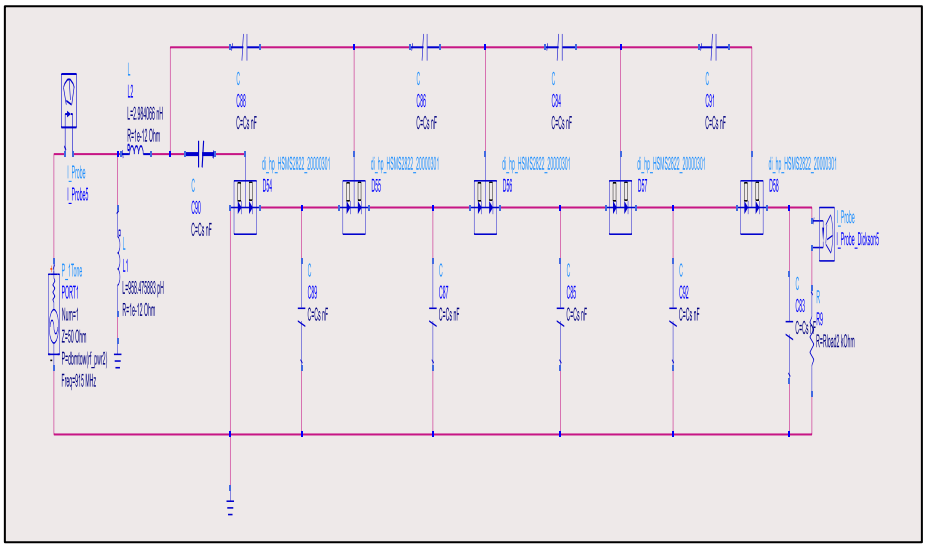


Figure 4.22. The five stages of DVM with L-matching impedance

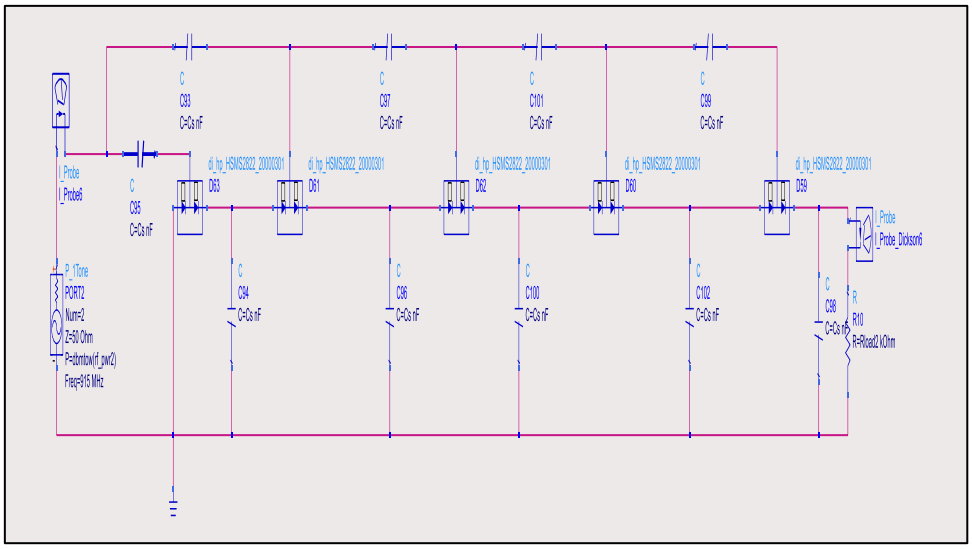
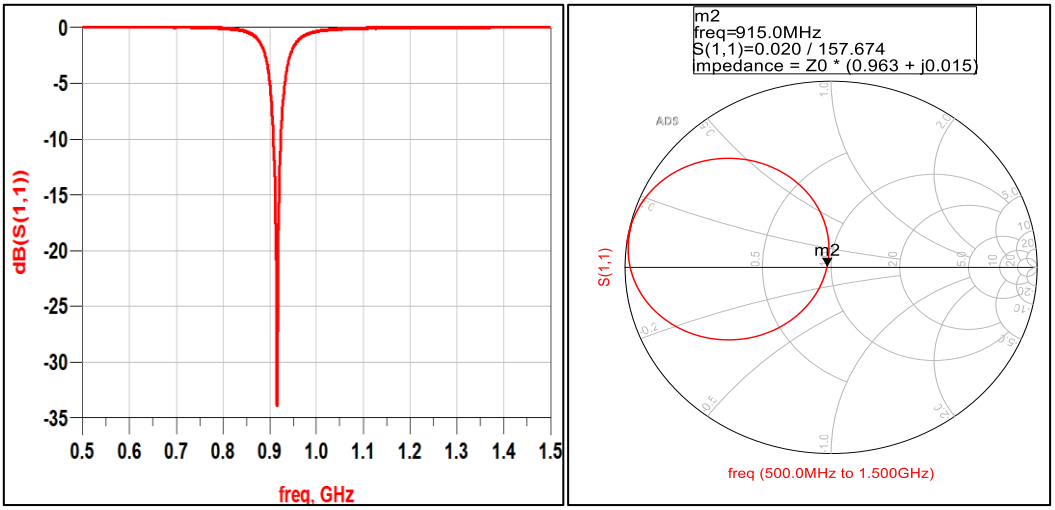


Figure 4.23. The five stages of DVM without matching impedance



(a) (b)

Figure 4.24. The $S_{(1,1)}$ the for fife stages of DVM with matching impedance

Figure 4.24(a). shows the $S_{(1,1)}$ for the five stages of DVM with matching impedance and the result of about -34.725 dB. Figure 4.24(b) shows the Smith chart of the matching impedance for 915 MHz that applied from 500 to 1500 MHz.

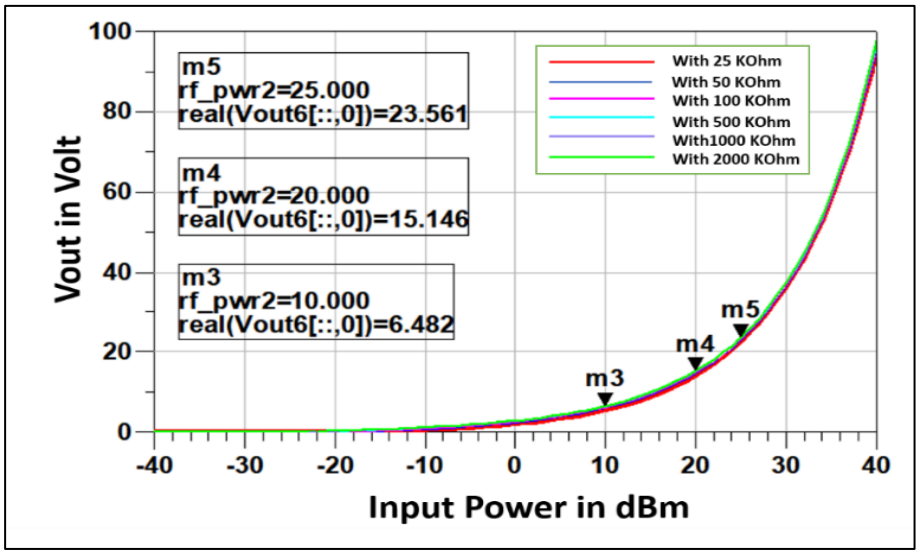


Figure 4.25. The V_{out} of 5-stages DVM using L matching impedance for HSMS 2822 diode

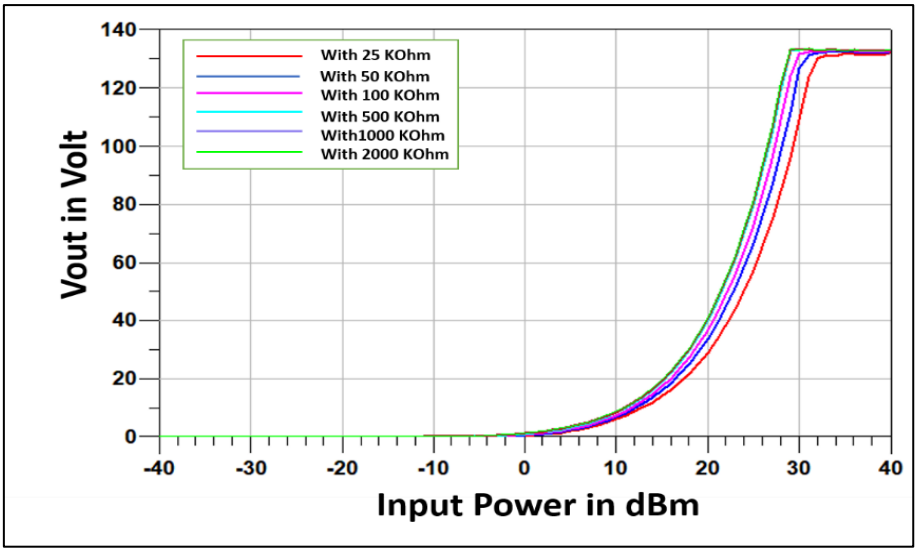


Figure 4.26. The V_{out} of 4-stages DVM without matching impedance for HSMS 2822 diode

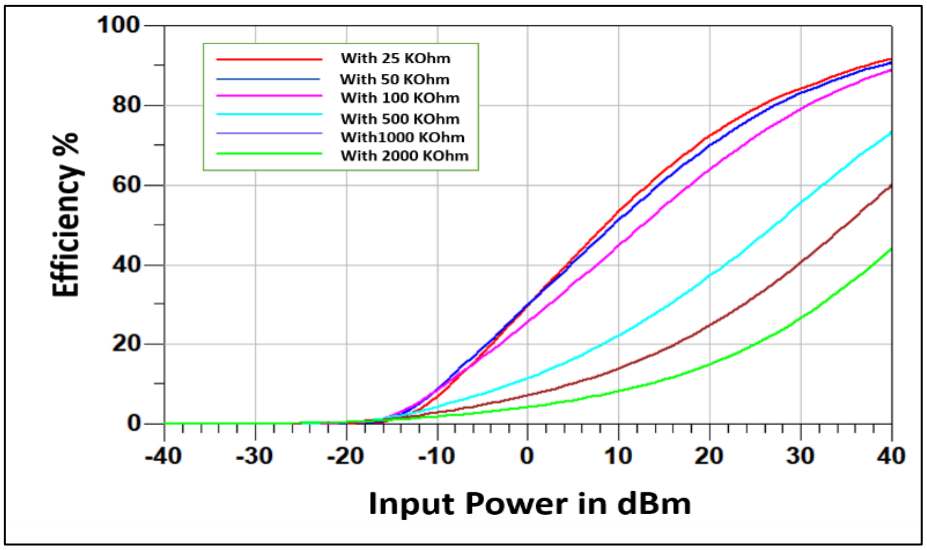


Figure 4.27. The efficiency of 5-stages DVM using L matching impedance for HSMS 2822 diode

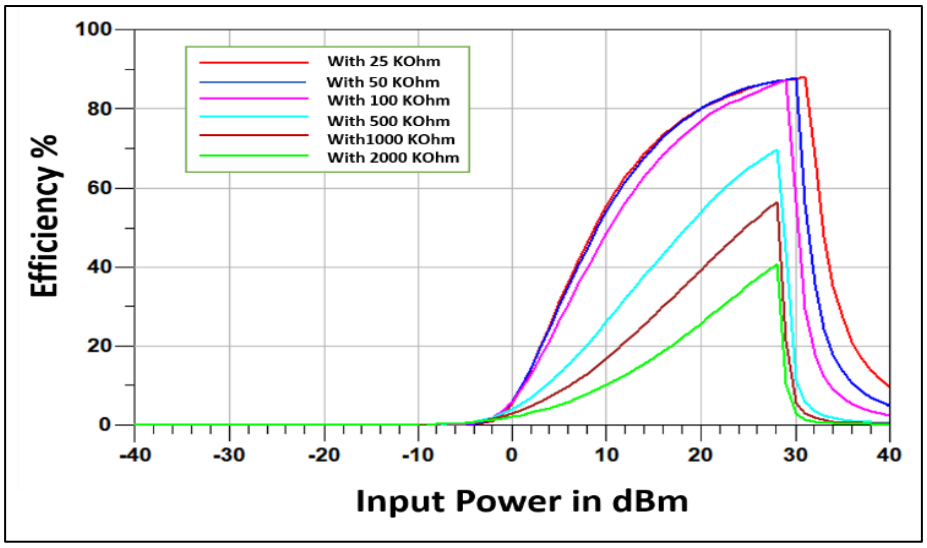


Figure 4. 28. The efficiency of 5-stages DVM without matching impedance for HSMS 2822 diode

E- the design of six stages for DVM

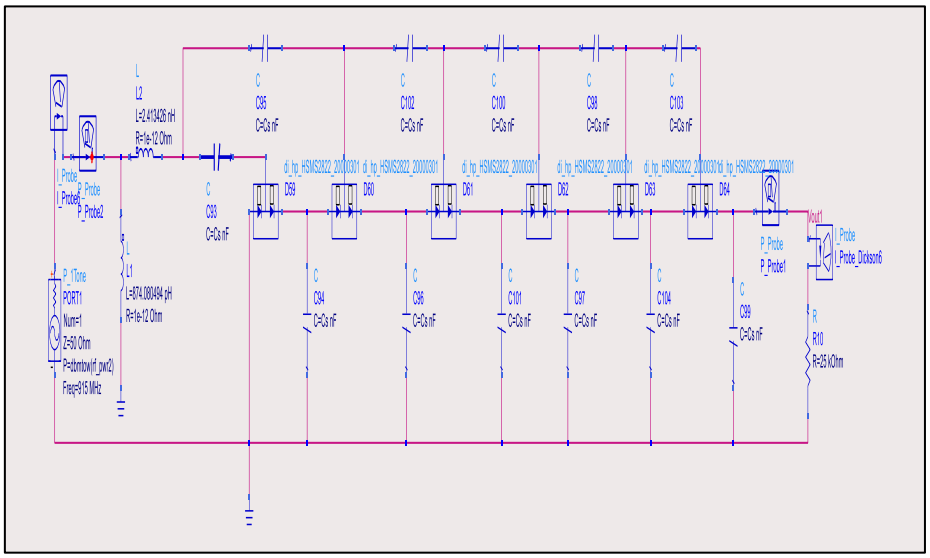


Figure 4.29. The six stages of DVM with L-matching impedance

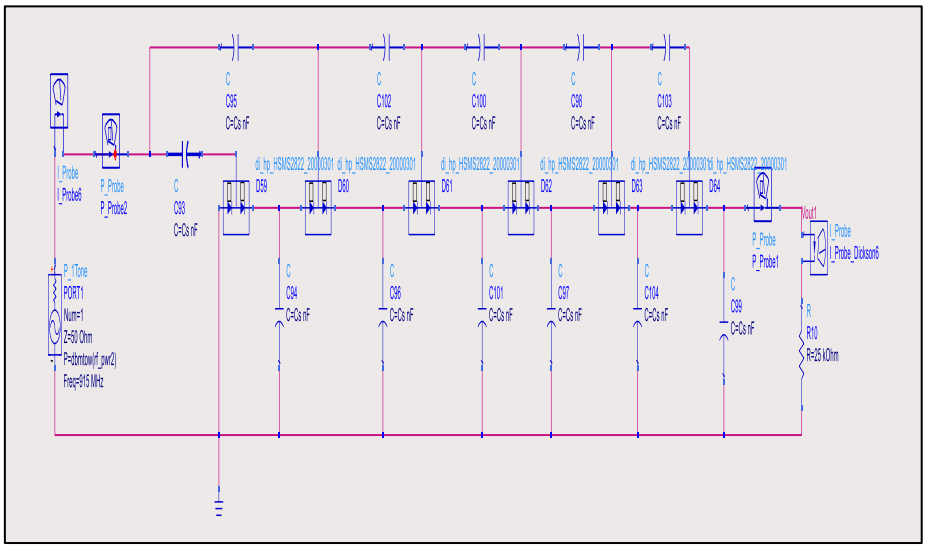
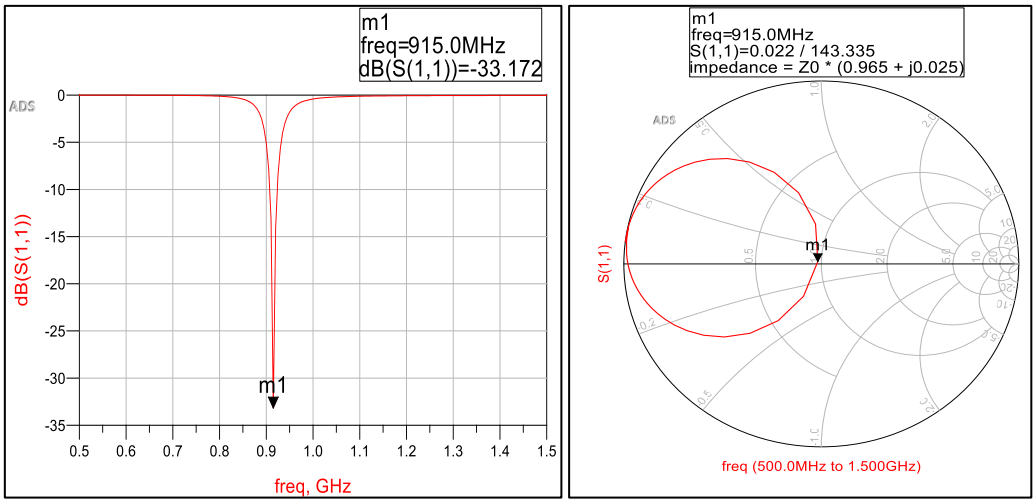


Figure 4.30. The six stages of DVM without matching impedance



(a) (b)

Figure 4. 31. The $S_{(1,1)}$ for the six stages of DVM with matching impedance

Figure 4.31(a). shows the $S_{(1,1)}$ for six stages of DVM with matching impedance and the result of about -33.172 dB. Figure 4.31(b) shows the Smith chart of the matching impedance for 915 MHz that applied from 500 to 1500 MHz.

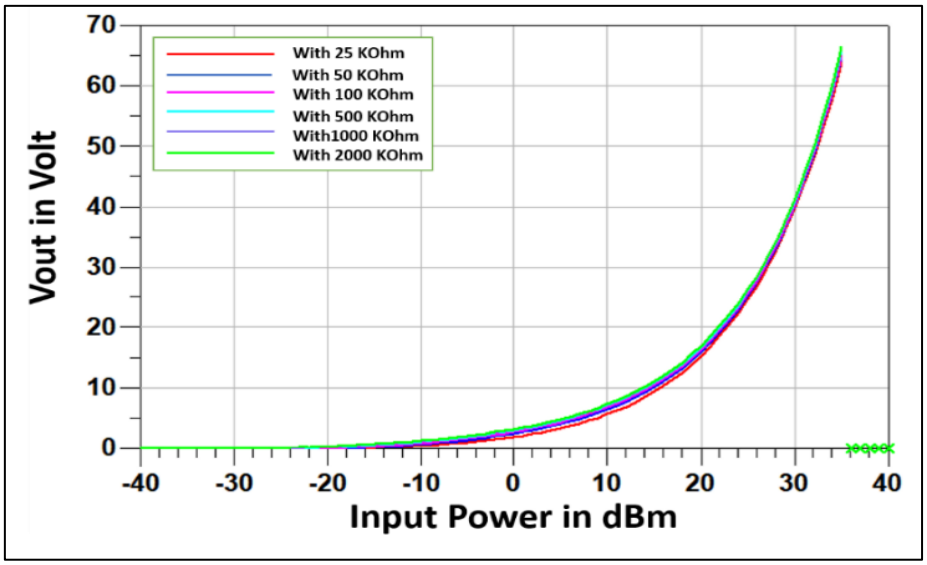


Figure 4. 32. The V_{out} of 6-stages DVM using L matching impedance for HSMS 2822 diode.

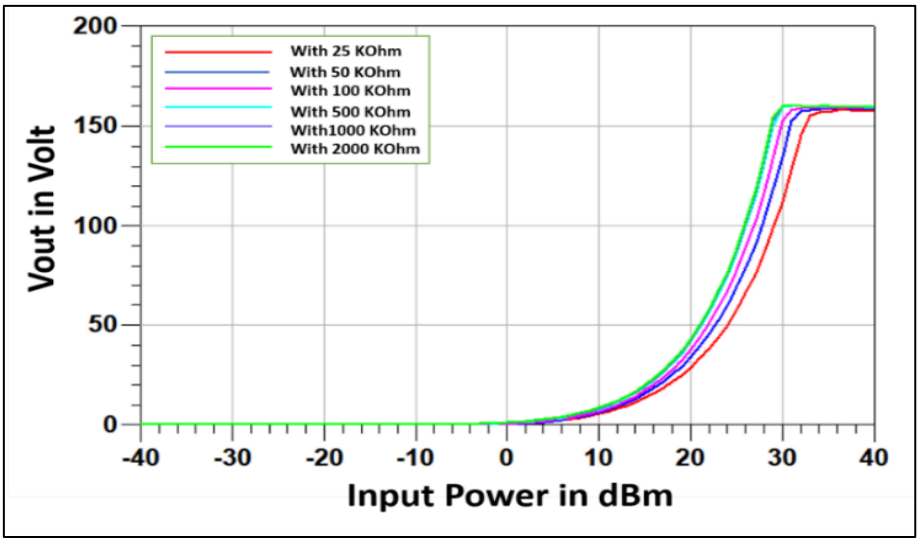


Figure 4. 33. The V_{out} of 6-stages DVM without matching impedance for HSMS 2822 diode

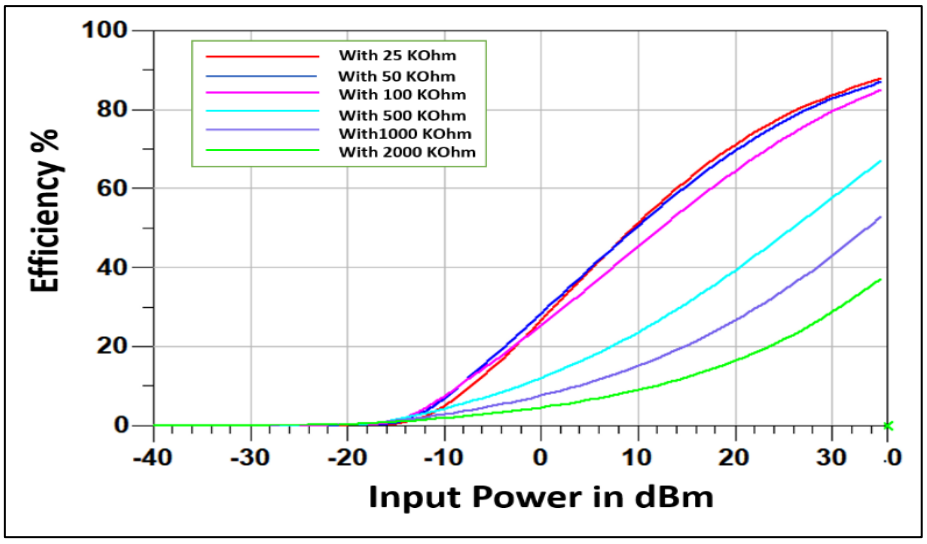


Figure 4. 34. The efficiency of 5-stages DVM using L matching impedance for HSMS 2822 diode

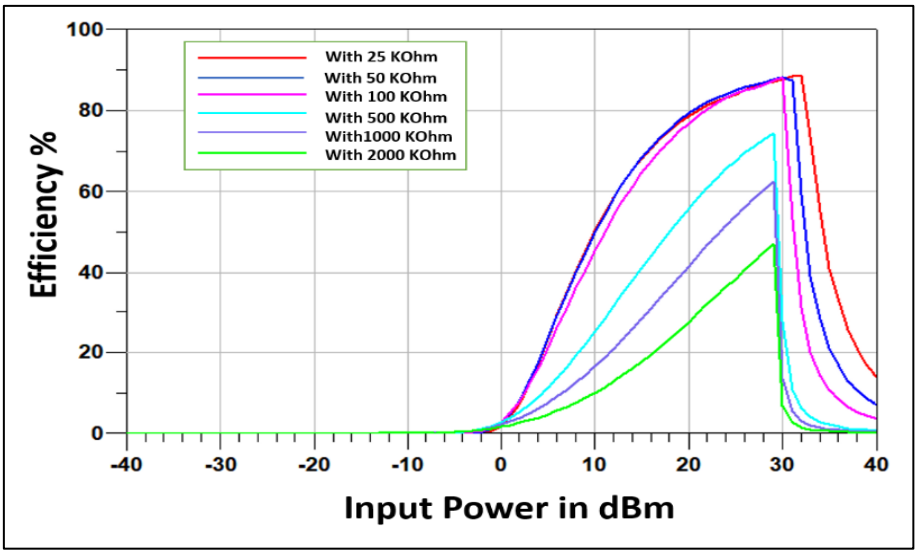


Figure 4. 35. The efficiency of 5-stages DVM without matching impedance for HSMS 2822 diode

Figure 4.32 shows the value of the output voltages using different load resistors with L matching impedance network for the period from -40 to 40 dBm. The simulation result shows the difference between the values of the voltages with the effect of the almost equal load resistances as the trend starts upward to reach the value of 100 Volts at 40 dBm. Figure 4.33. The value of the output voltages without using the L matching impedance network shows that the outputs of the circuit started from the period -3 dBm, unlike the previous figure, and the output values began to increase, reaching a value of approximately 35 volts in 20 dBm and a value of 130 volts in 30 dBm. Figure 4.34 shows the efficiency value of the circuit using L-matching impedance. The results show that the efficiency value changes with the change in the load value. The highest efficiency value of the circuit that can be obtained with the lowest value of the load is 25 KΩ, which reaches 88.5%, and the lowest efficiency value is 42% when the resistance value is 2000 KΩ. Figure 4.35. It is described showing the efficiency value of the circuit using L matching impedance, and the results show that the efficiency value changes with the change in the load value as well, but with fewer values than the previous figure.

4.2.2. The DVM Design With T Matching

A- the design of two stages for DVM

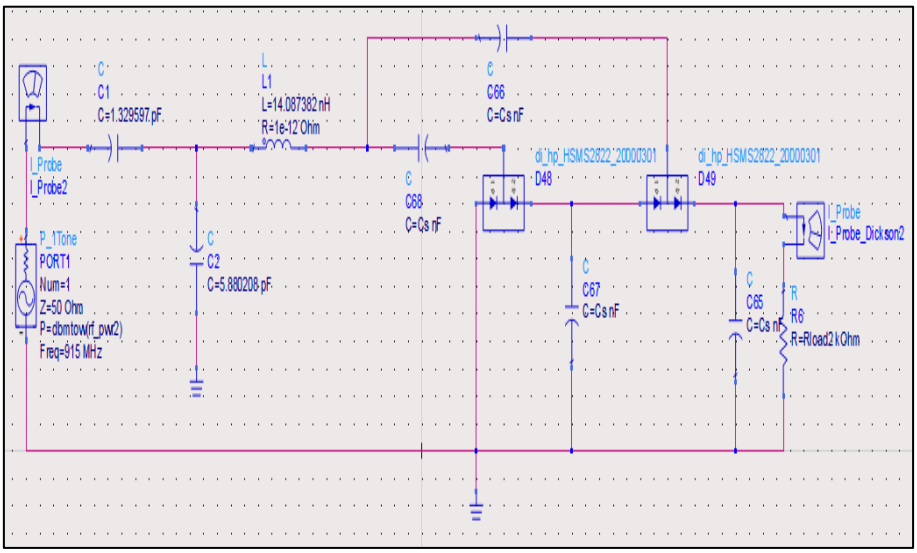


Figure 4. 36. The two stages of the DVM circuit with T-matching impedance

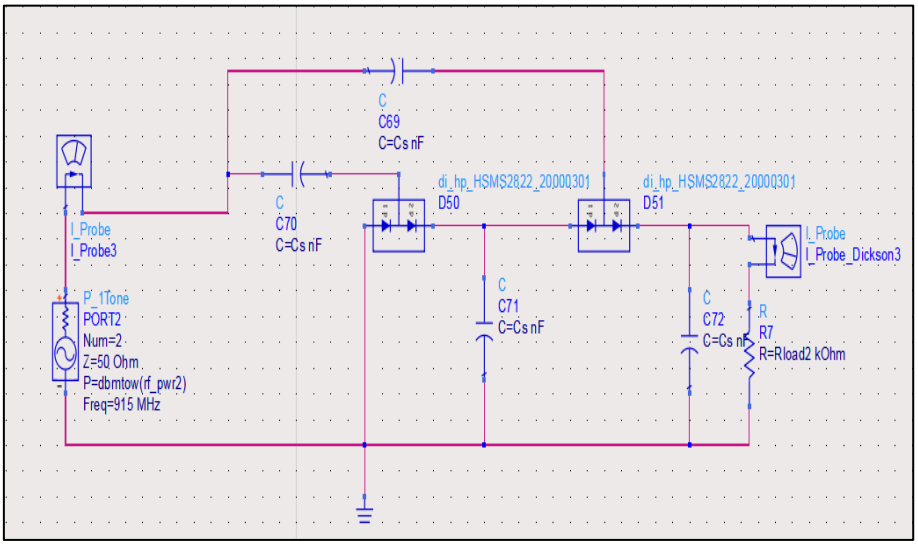
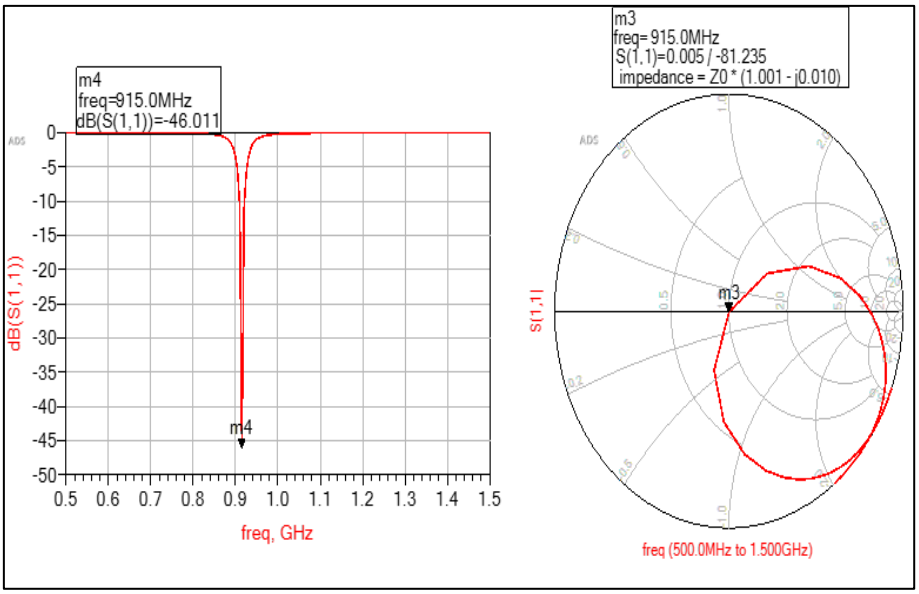


Figure 4.37. The two stages of the DVM circuit without matching impedance



(a) (b)

Figure 4. 38. The $S_{(1,1)}$ for the two stages of DVM with matching impedance

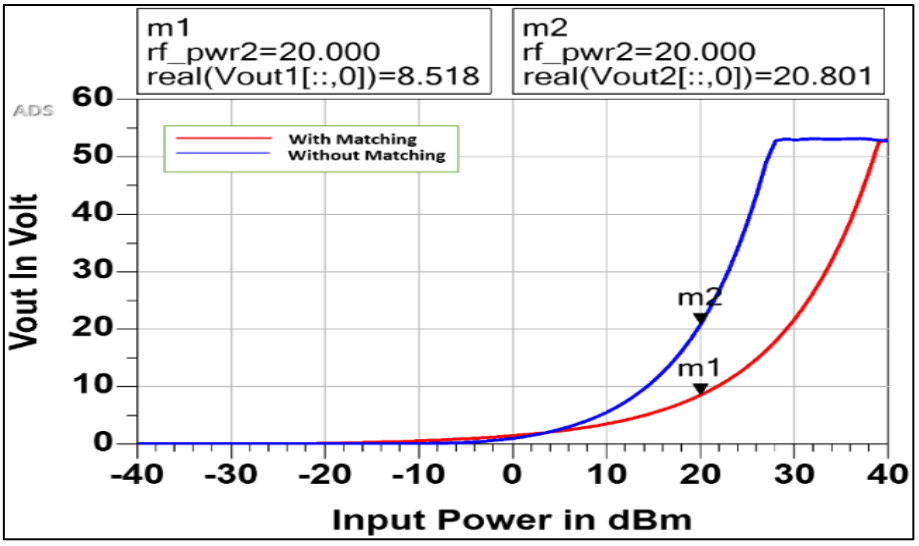


Figure 4. 39. The V_{out} of 2-stages DVM with and without T matching impedance for HSMS 2822 diode.

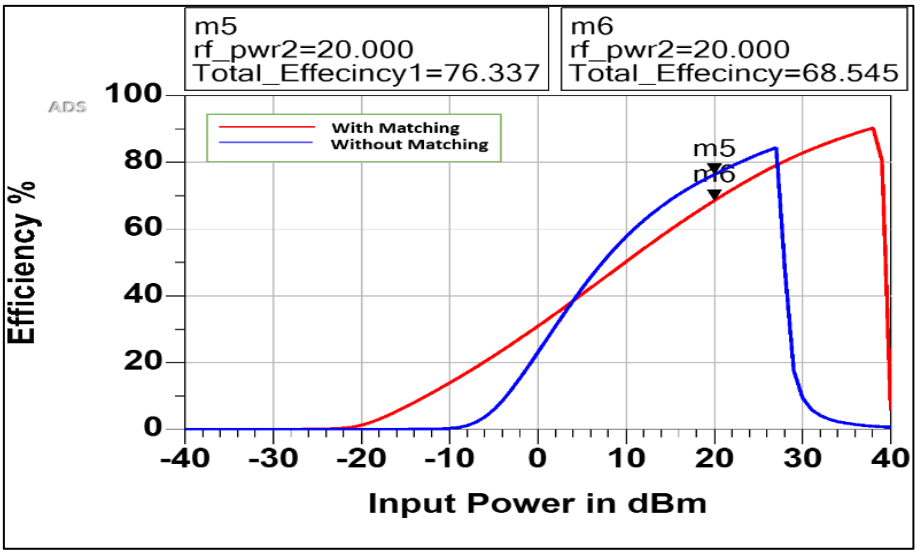


Figure 4. 40. The efficiency of 2-stages DVM with and without T matching impedance for HSMS 2822 diode.

B- the design of six stages for DVM

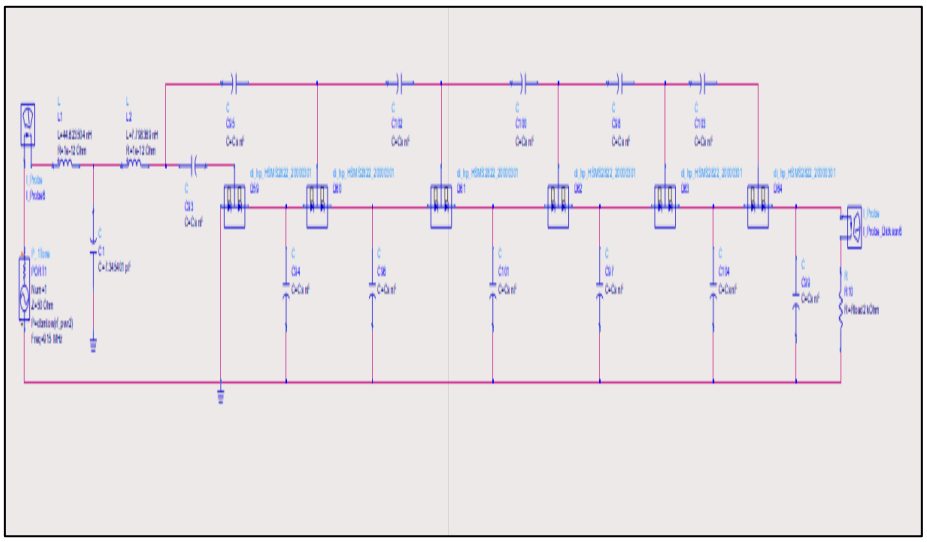


Figure 4.41. The two stages of the DVM circuit with T-matching impedance

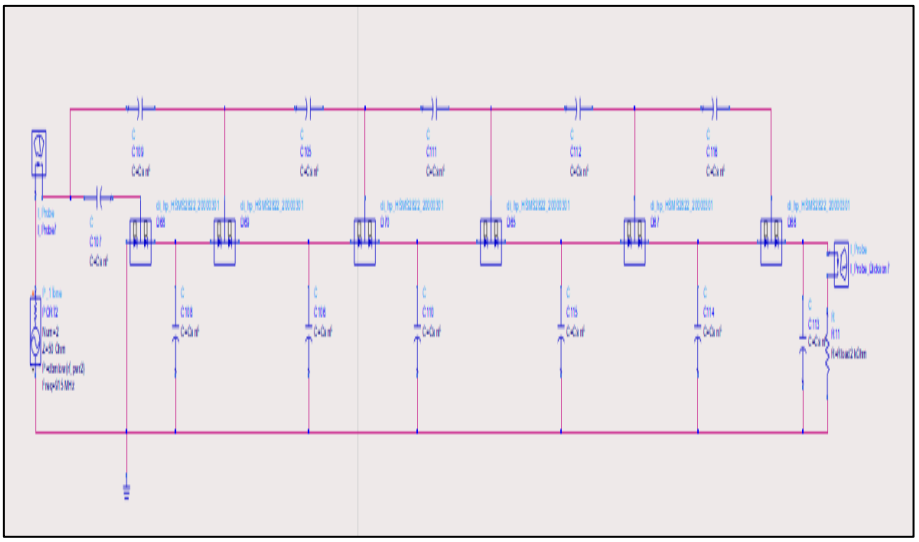
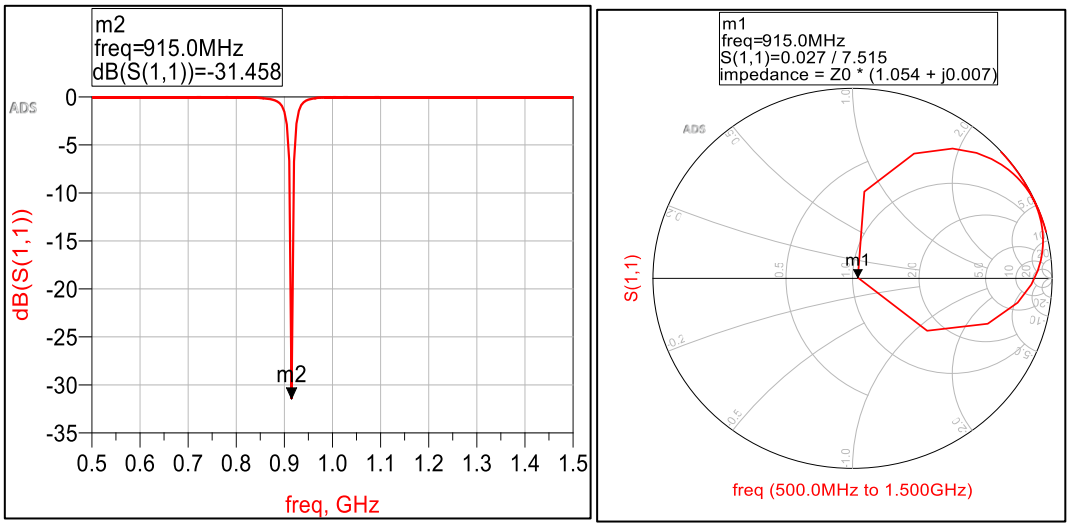


Figure 4.42. The two stages of the DVM circuit without matching impedance



(a) (b)

Figure 4. 43. The $S_{(1,1)}$ for the six stages of DVM with matching impedance.

Figure 4.43 a. shows the $S_{(1,1)}$ for six stages of DVM with T matching impedance, which results in about -31.458 dB. Figure 4.43 b shows the Smith chart of the matching impedance for 915 MHz that was applied from 500 MHz to 1500 MHz.

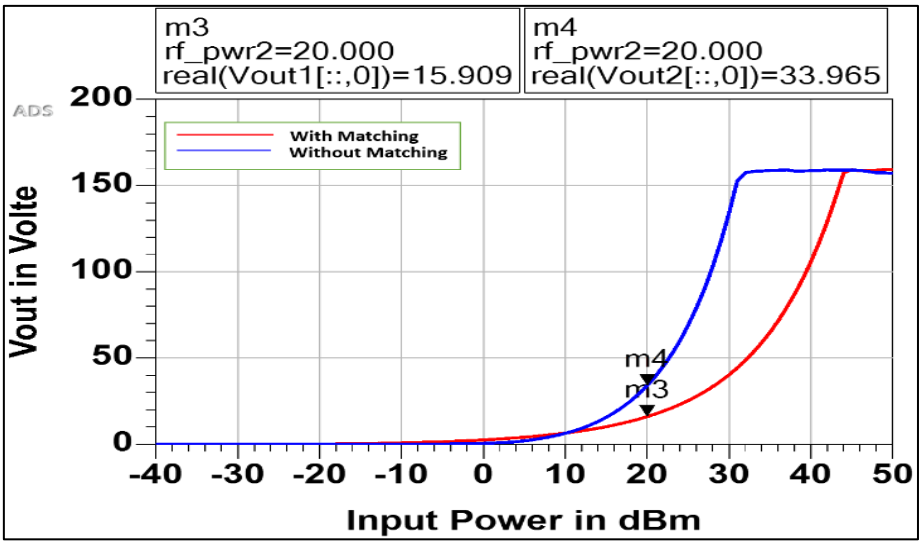


Figure 4.44. The V_{out} of 6-stages DVM with and without T matching impedance for HSMS 2822 diode

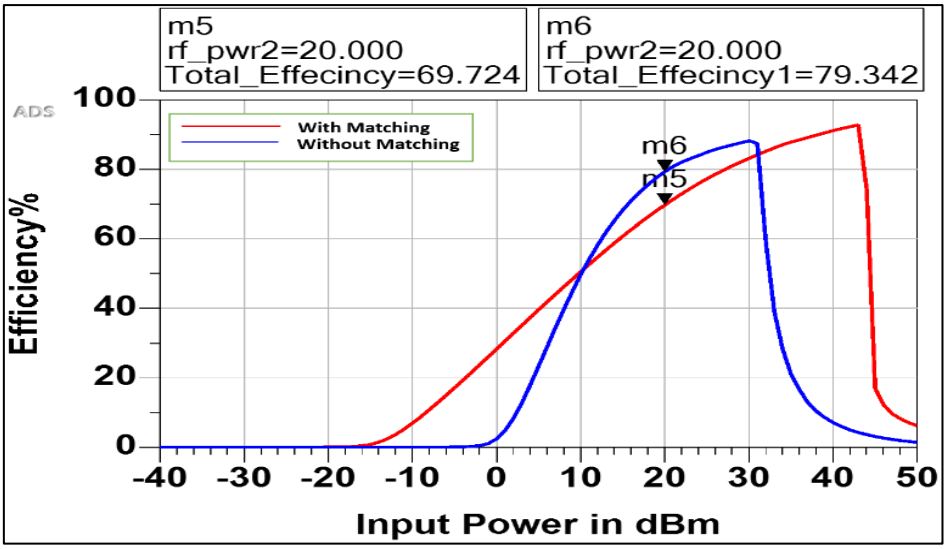


Figure 4.45. The efficiency of 6-stages DVM with and without T matching impedance for HSMS 2822 diode

Figure 4.44 shows the simulation/result of the Vout for the 6-stages DVM by applying the T matching network. The result indicates that voltages started to rise from -10 dBm with matching impedance to 0 dBm without matching impedance. To make a comparison, two points have been selected for both simulations at 20 dBm. The circuit with a matching impedance and greater coverage gives a broader range of input power and high stability. Figure 4.45 shows the efficiency of the DVM with and without using the matching impedance network, and the result indicates that with the use of the

matching impedance network, the efficiency scheme covers a range with an increase in the efficiency value and high stability.

4.2.3. The Dvm Design With π Matching

A- the design of two stages for DVM

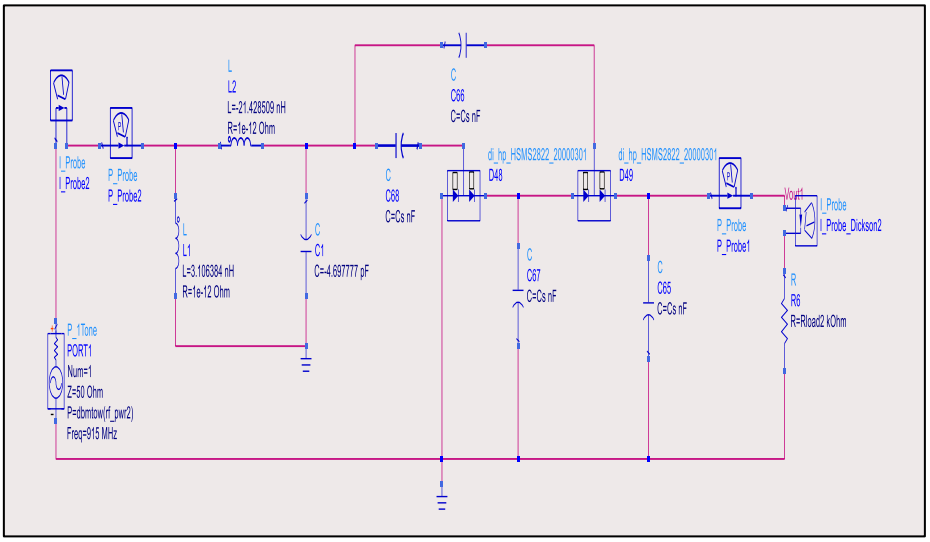


Figure 4.46. The two stages of the DVM circuit with π matching impedance

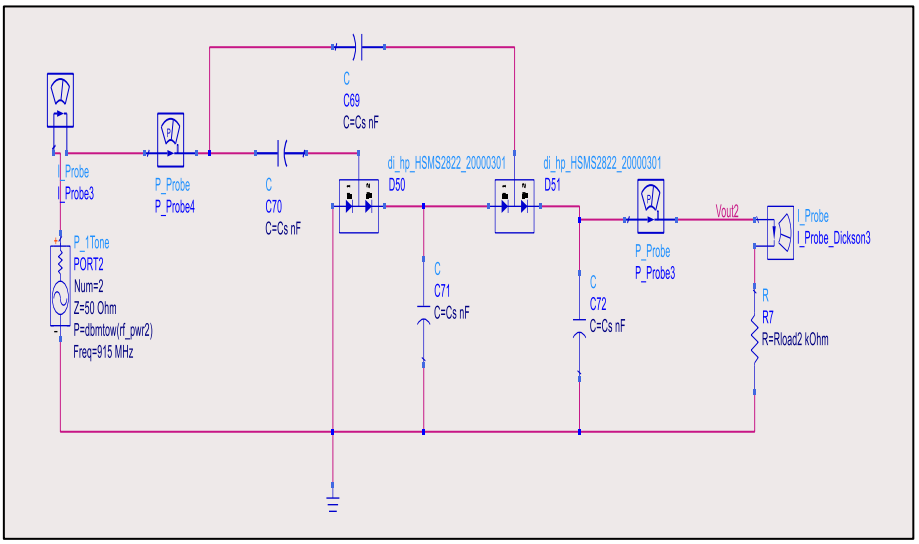


Figure 4.47. The two stages of the DVM circuit without π matching impedance

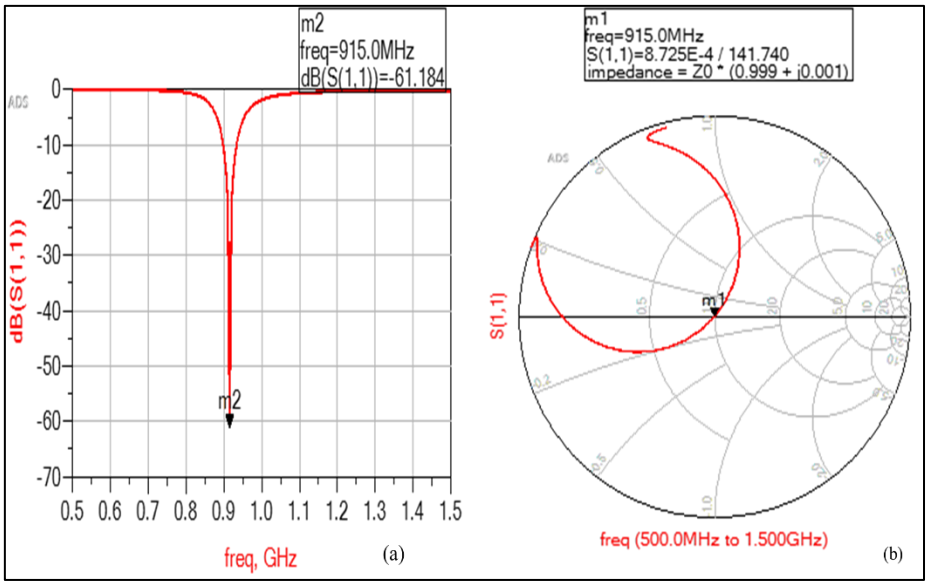


Figure 4.48. The $S_{(1,1)}$ the two stages of DVM with π matching impedance.

Figure 4.48 a. shows the $S_{(1,1)}$ for two stages of DVM with π matching impedance and the result of about -61.184 dB. Figure 4.48 b shows the Smith chart of the matching impedance for 915 MHz that was applied from 500 MHz to 1500 MHz.

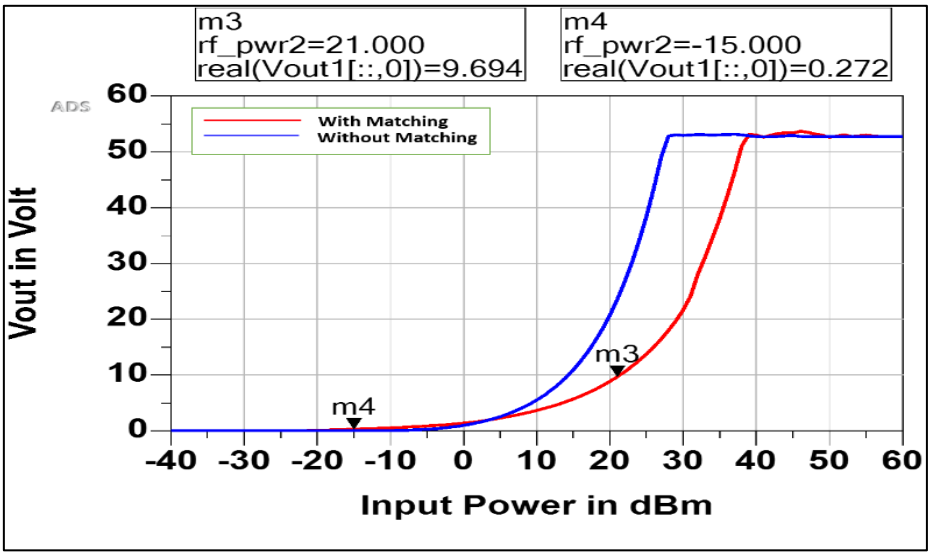


Figure 4.49. The V_{out} of 2-stages DVM with and without π matching impedance for HSMS 2822 diode

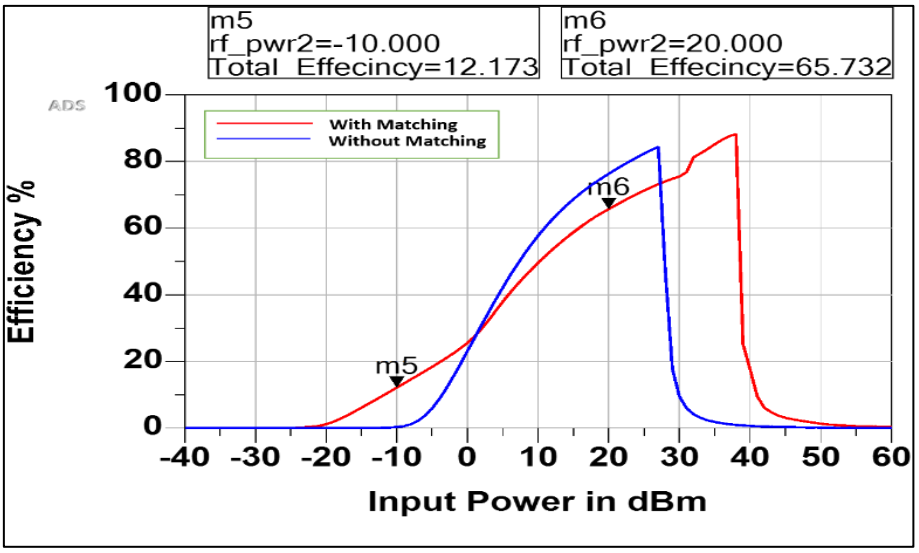


Figure 4.50. The efficiency of 2-stages DVM with and without π matching impedance for HSMS 2822 diode

Figure 4.49 The output/voltage for the two stages of DVM with and without π matching impedance network. Besides, in the simulation to test the functionality of the system to points has been selected, m4= 0.297V at -15 dBm, where its 0 at the same input power without using matching impedance, and m3=9.694 at 20 dBm for the line of π matching simulation. Also, the result shows the activity using a matching impedance network. In addition, Figure 4.50 shows the efficiency of two stages of DVM with and without π by applying different load conditions, and the result shows that the efficiency scheme covers a range with an increase in the efficiency value and high stability using the matching impedance.

B- The design of six stages for DVM

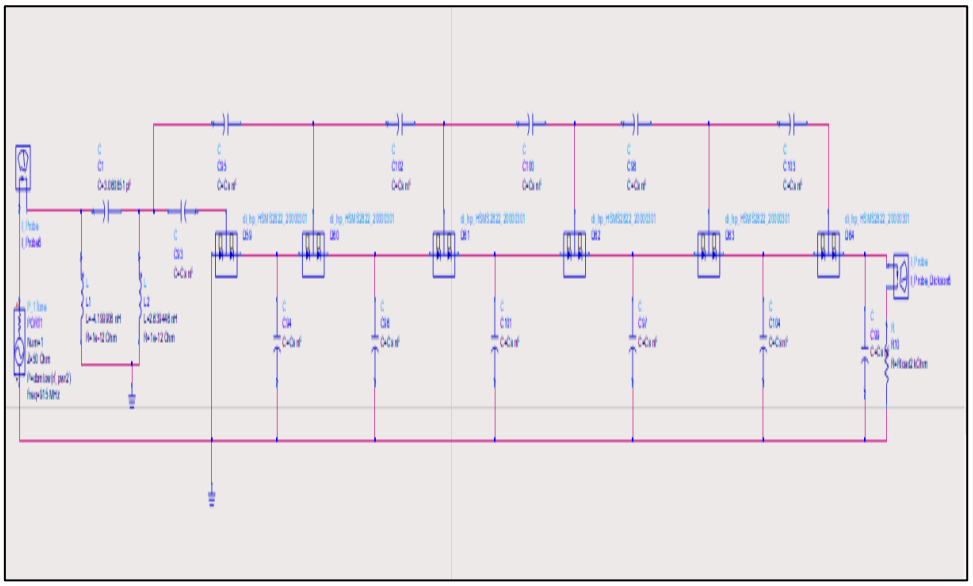


Figure 4.51. The six stages of the DVM circuit with π matching impedance

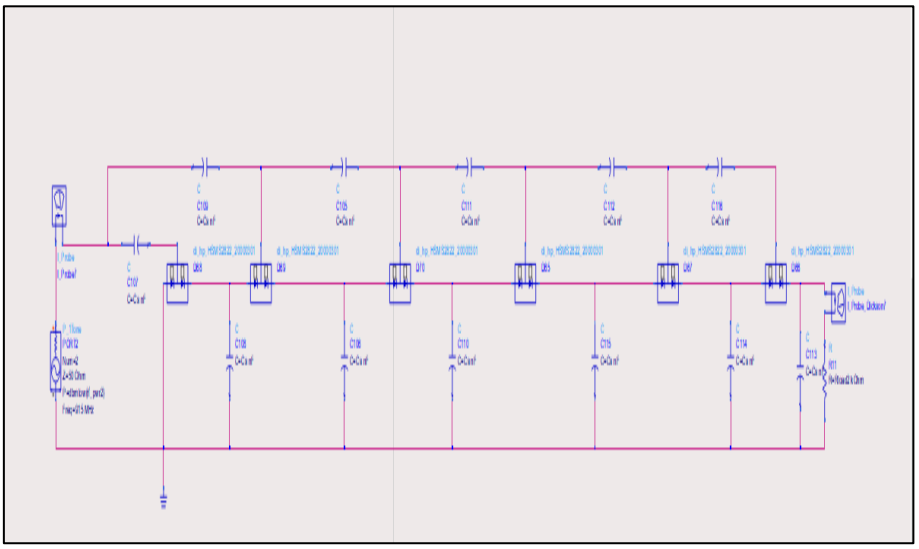


Figure 4.52. The six stages of the DVM circuit without π matching impedance

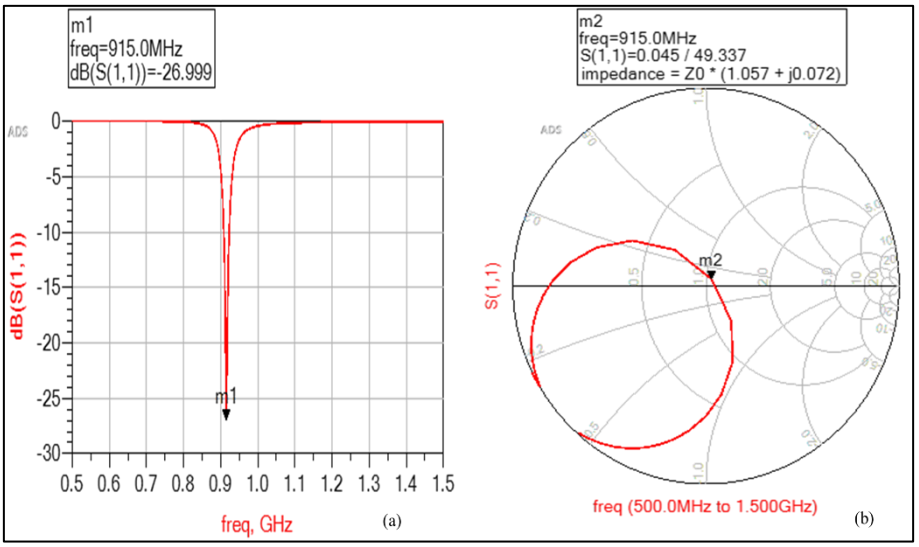


Figure 4.53. The $S_{(1,1)}$ the six stages of DVM with π matching impedance.

Figure 4.53(a). shows the $S_{(1,1)}$ for six stages of DVM with π matching impedance and the result of about -26.999 dB. Figure 4.53(b) explains the Smith chart of the matching impedance for 915 MHz that applied from 500 to 1500 MHz.

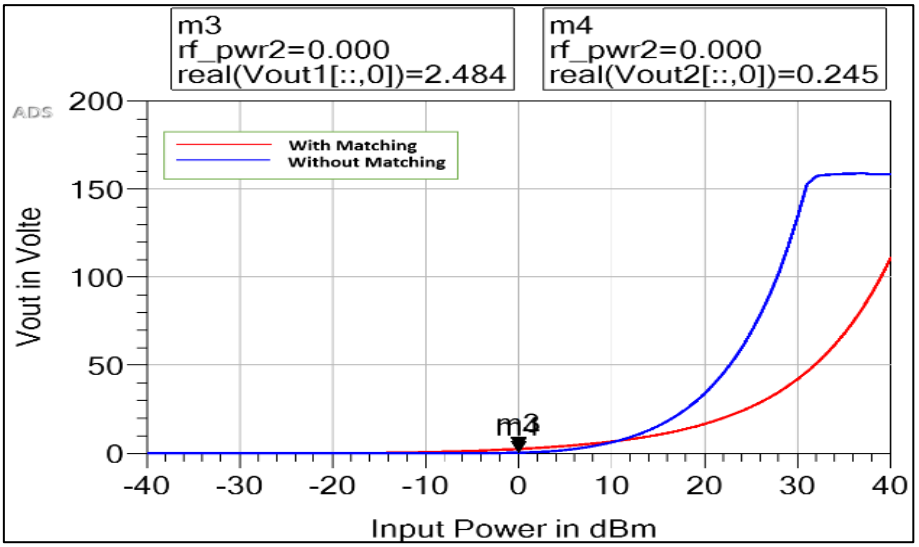


Figure 4.54. The V_{out} of 2-stages DVM with and without π matching impedance for HSMS 2822 diode

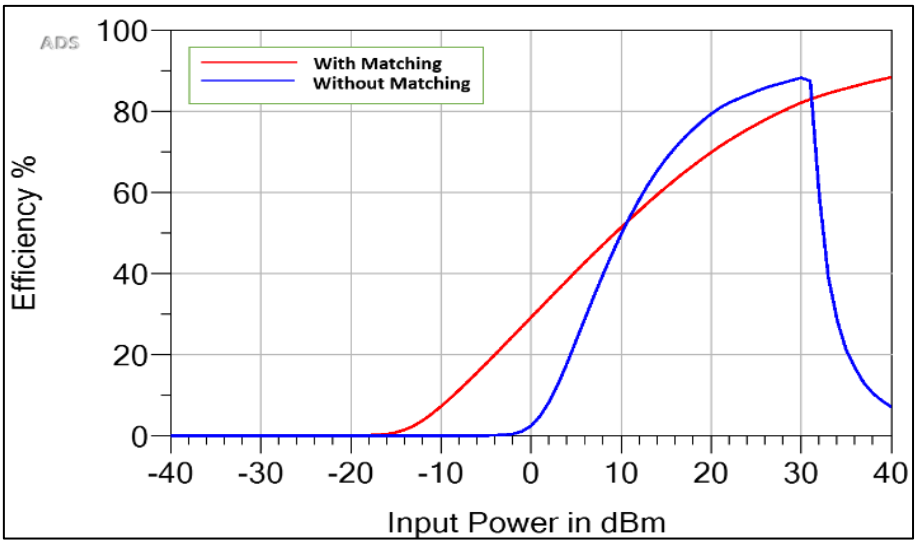


Figure 4.55. The efficiency of 6-stages DVM with and without π matching impedance for HSMS 2822 diode

In this part, the same idea to test the systems has been applied in the simulation with different conditions to test the effect and stability of DVM with and without using matching impedance. According to Figure 4.54, which represents the Vout of the circuit and also two points have been selected at 0 dBm, which are m3 for the line with matching and m4 for the line without matching, and the result shows the circuit with matching impedance has a wide range and highest Vout value than without using matching impedance. In addition, the efficiency test has been applied in Figure 4.55 with the same conditions applied in Figure 4.50. The result shows that the efficiency scheme covers a range with increased efficiency value and high stability using the matching impedance.

4.3. THE HARVESTING CIRCUIT FOR HSMS 2850 DIODE

In this part, the circuits of DVM will be designed and tested by using an HSMS 2850 diode operating at a frequency of 915 MHz. In this section, DVM circuits will be developed at different stages from 2 to 6 and apply three different matching impedance topologies, L, T, and π matching networks. Each circuit will be simulated individually to test the Vout and the efficiency, and the results will discuss in detail.

4.3.1. The DVM Design With L Matching

In this section, as shown in Figure 4.56, the DVM circuits from 2 to 6 stages will be designed and simulated by applying L matching in one window at once. Each time the load resistance types (25, 50, 100, 500, 1000, and 2000 KΩ) will be changed and applied to the entire group to study and analyze the outputs for both efficiency and voltage. The effect of the number of stages in the DVM on the values of each of the voltages and the equivalent will be studied and analyzed.

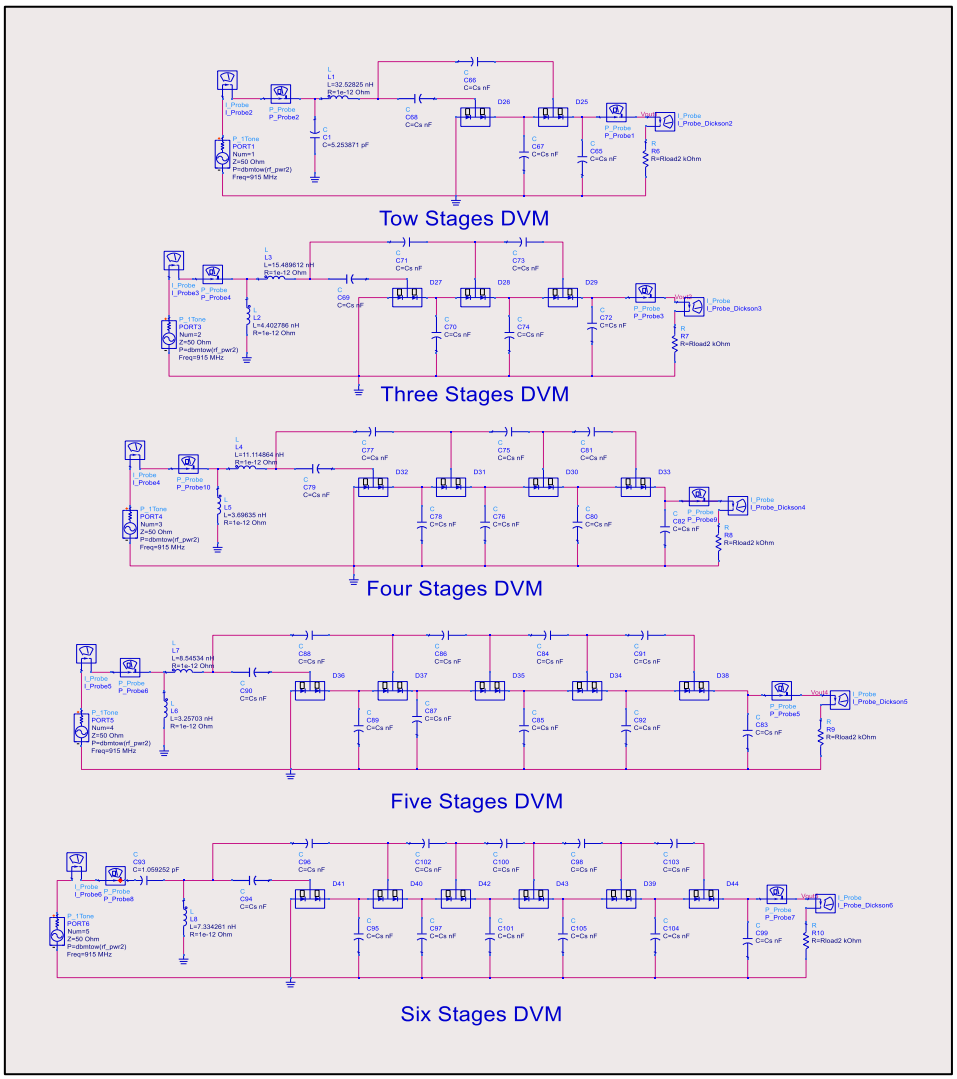


Figure 4.56. The stages of DVM circuits with *L* matching impedance

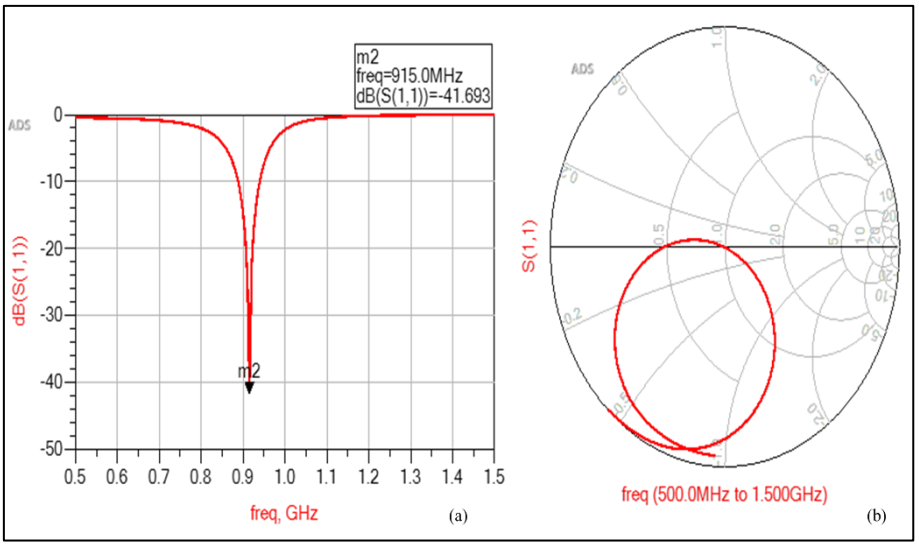


Figure 4.57. The $S_{(1,1)}$ for the two stages of DVM with *L* matching impedance.

Figure 4.57(a). shows the $S_{(1,1)}$ for two stages of DVM with *L* matching impedance and the result of about -41.693 dB. Figure 4.57(b) shows the Smith chart of the matching impedance for 915 MHz applied from 500 to 1500 MHz.

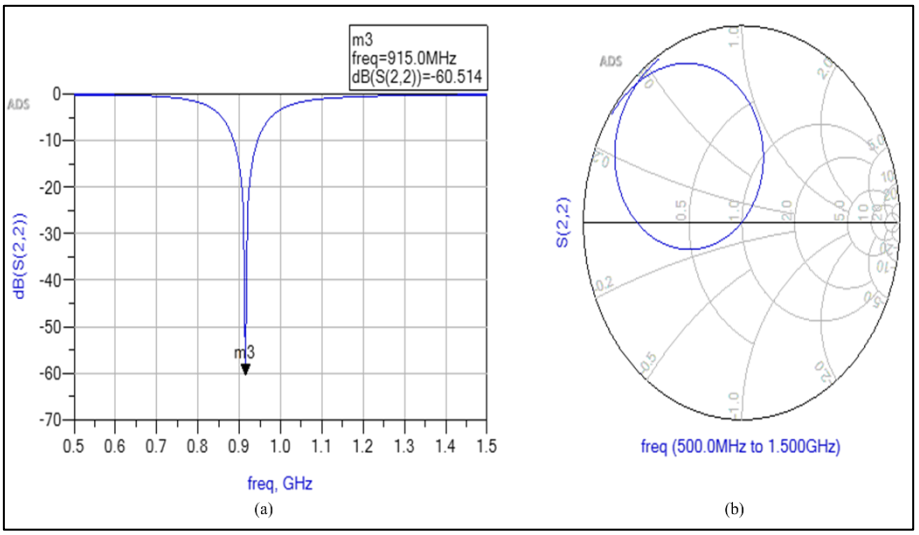


Figure 4.58. The $S_{(1,1)}$ for two stages of DVM with *L* matching impedance.

Figure 4.58(a). shows the $S_{(1,1)}$ for three stages of DVM with *L* matching impedance and the result of about -60.451 dB. Figure 4.58(b) shows the Smith chart of the matching impedance for 915 MHz that applied from 500 to 1500 MHz.

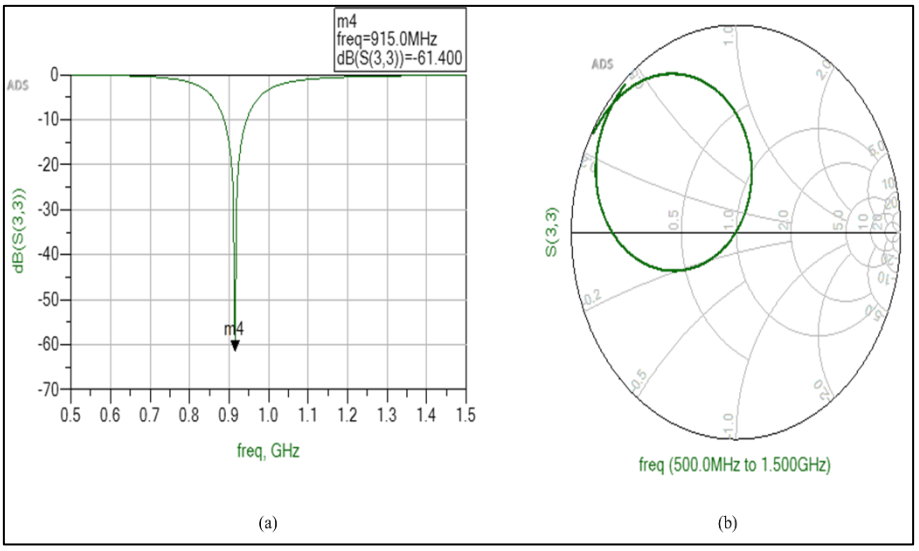


Figure 4.59. The $S_{(1,1)}$ for the two stages of DVM with *L* matching impedance.

Figure 4.59(a). shows the $S_{(1,1)}$ for four stages of DVM with *L* matching impedance and the result of about -61.400 dB. Figure 4.45(b) shows the Smith chart of the matching impedance for 915 MHz that applied from 500 to 1500 MHz.

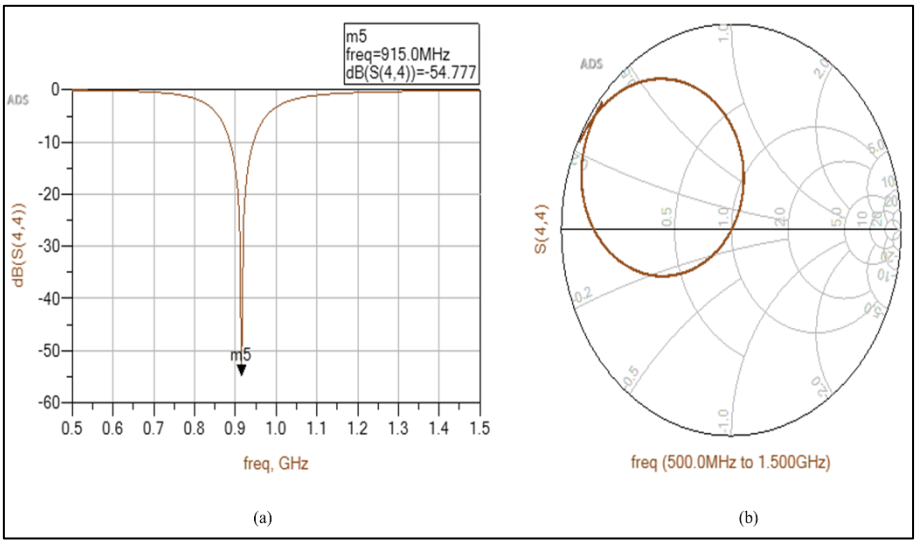


Figure 4.60. The $S_{(1,1)}$ for the five stages of DVM with *L* matching impedance.

Figure 4.60(a). shows the $S_{(1,1)}$ for five stages of DVM with *L* matching impedance and the result of about -54.777 dBm. Figure 4.60(b) shows the Smith chart of the matching impedance for 915 MHz applied from 500 to 1500 MHz.

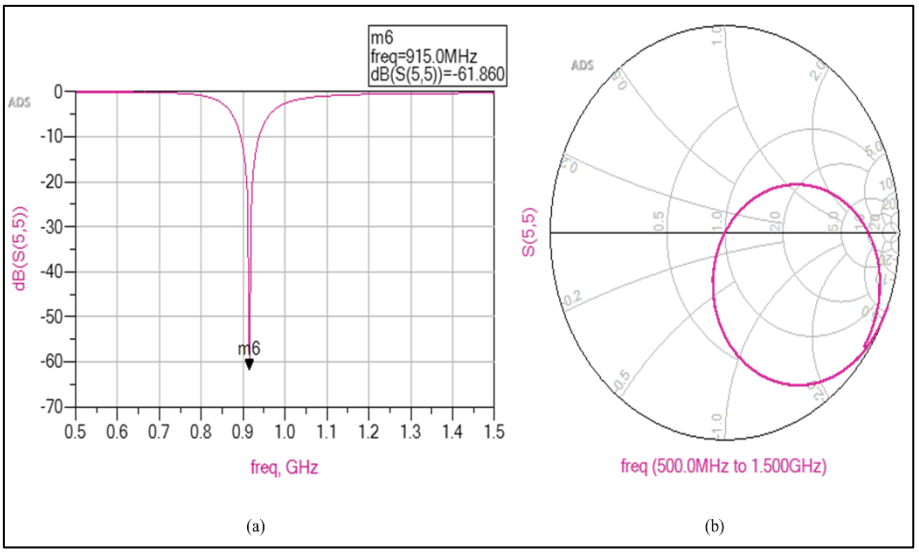


Figure 4.61. The $S_{(1,1)}$ for the six stages of DVM with *L* matching impedance.

Figure 4.61(a). shows the $S_{(1,1)}$ for six stages of DVM with *L* matching impedance and the result of about -61.860 dB. Figure 4.61(b) shows the Smith chart of the matching impedance for 915 MHz applied from 500 to 1500 MHz.

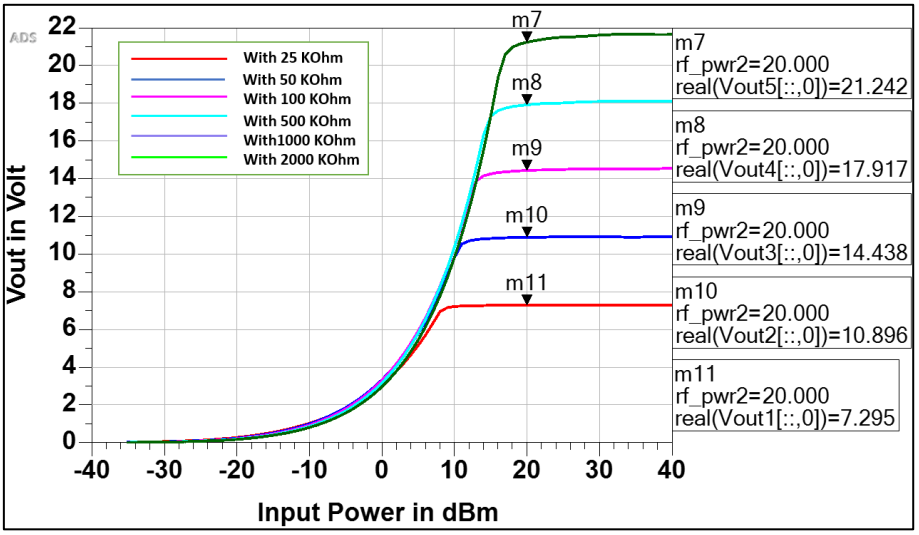


Figure 4.62. The V_{out} of two stage DVM using L matching impedance for HSMS 2850 diode at 25, 50, and 100 KΩ of load conditions.

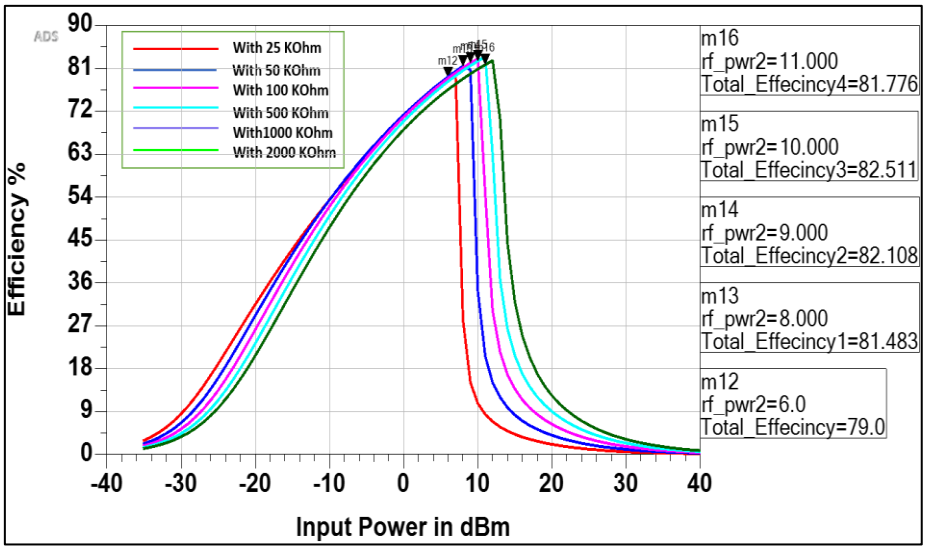


Figure 4.63. The efficiency of two-stage DVM using L matching impedance for HSMS 2822 diode at 25, 50, and 100 KΩ of load conditions.

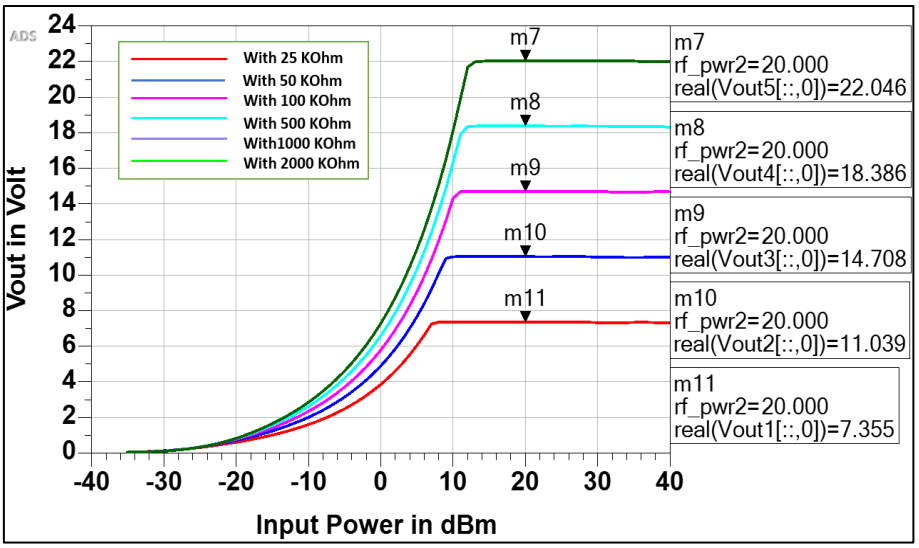


Figure 4.64. The V_{out} of two stage DVM using L matching impedance at 500 KΩ of load conditions

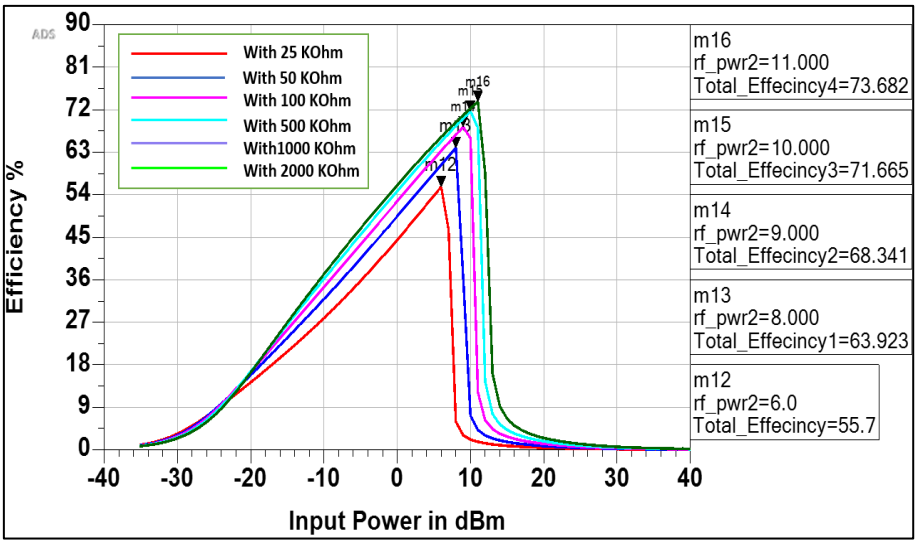


Figure 4.65. The efficiency of 2-stage DVM using L matching impedance at 500 KΩ of load conditions.

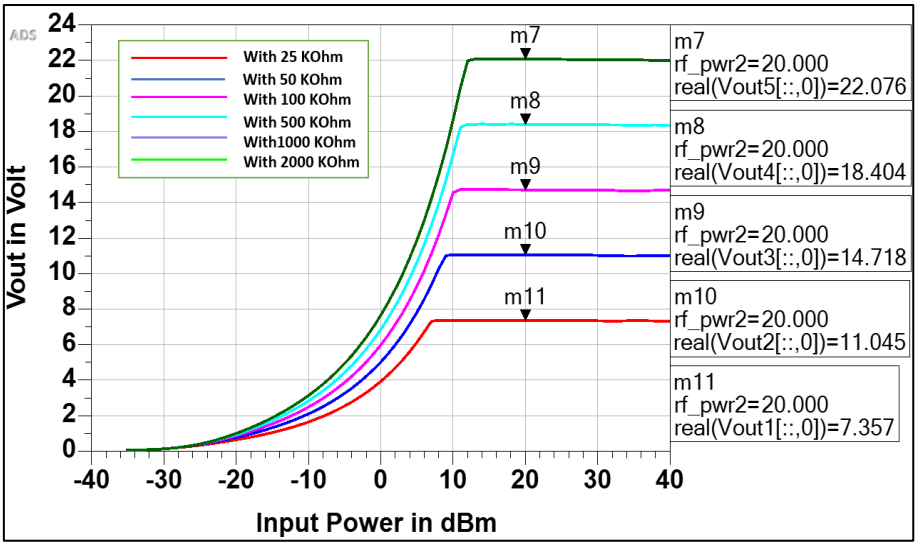


Figure 4.66. The V_{out} of two stage DVM using L matching impedance at 1000 and 2000 KΩ of load conditions.

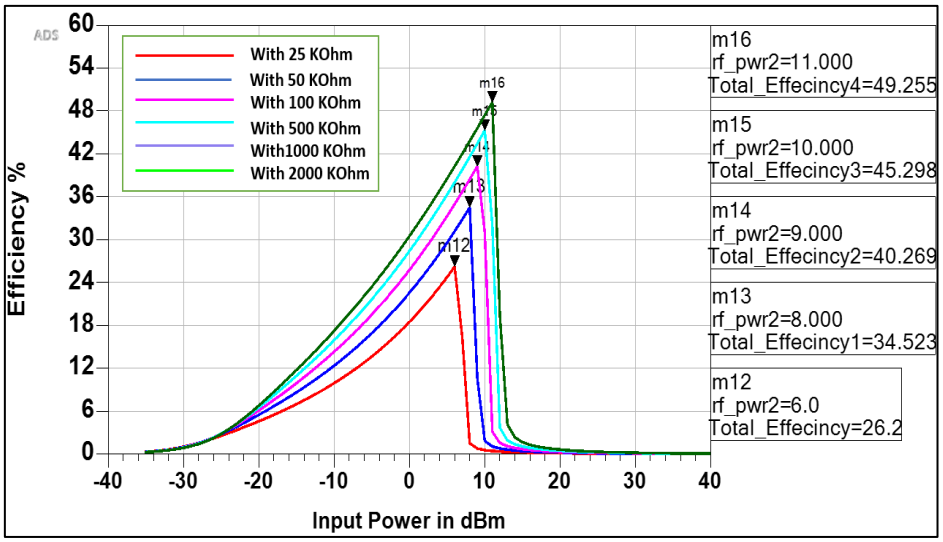


Figure 4.67. The efficiency of 2-stage DVM using L matching impedance at 500 KΩ of load conditions at 1000 and 2000 KΩ of load conditions

At the simulation result, different load conditions are applied for each DVM circuit: (25, 50, 100, 500, 1000, and 2000 to 2500 kΩ). Figures 4.62, 4.64, and 4.66 represent the Vouts of DVM. Therefore, the simulation results show that the Vout values are almost constant and don't affect load changes. In the same simulation, figures 4.63, 4.65, and 4.67 represent the efficiency of DVM by applying the same load conditions, and the results show that the efficiency of DVM is affected by the change of load resistance. Hence, The efficiency value is at its highest value when the load resistance affecting the circuit is in the smallest value or proportion to the circuit design.

4.3.2. The DVM Design With T Matching

A- The design of two and six stages for DVM Circut using T matching

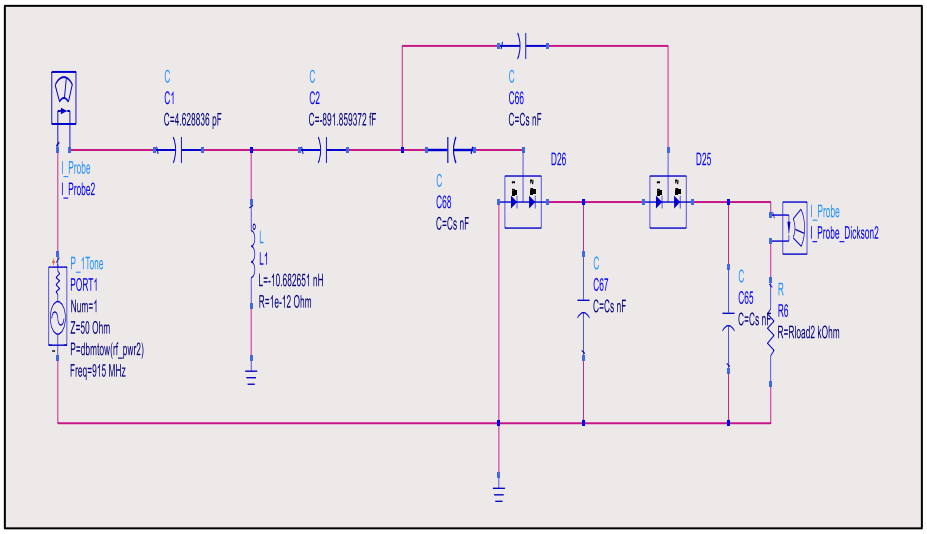


Figure 4.68. The two stages of the DVM circuit with T-matching impedance

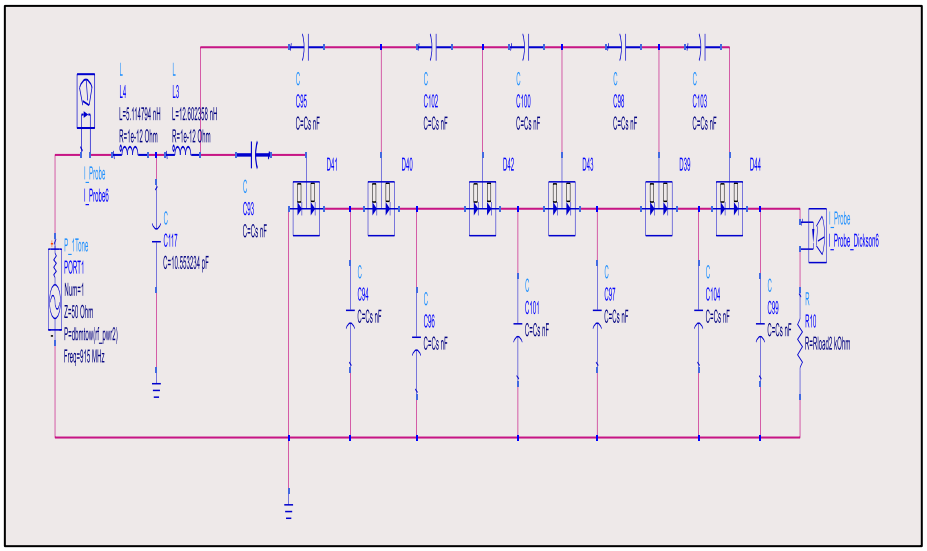


Figure 4.69. The six stages of the DVM circuit with T-matching impedance

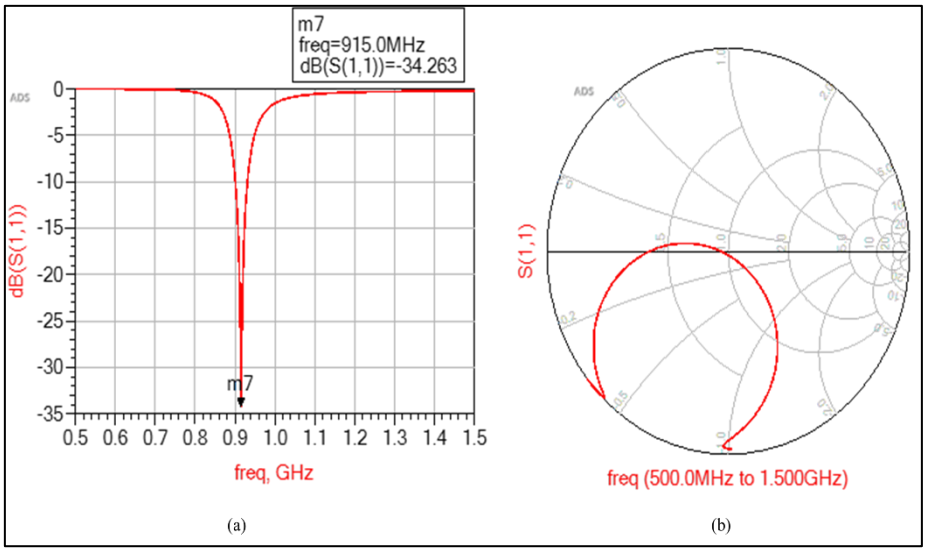


Figure 4.70. The $S_{(1,1)}$ for the two stages of DVM with T matching impedance.

Figure 4.70(a) shows the $S_{(1,1)}$ for six stages of DVM with *L* matching impedance and the result of about -34.263 dB. Figure 4.70(b) shows the Smith chart of the T matching impedance for 915 MHz that applied from 500 to 1500 MHz.

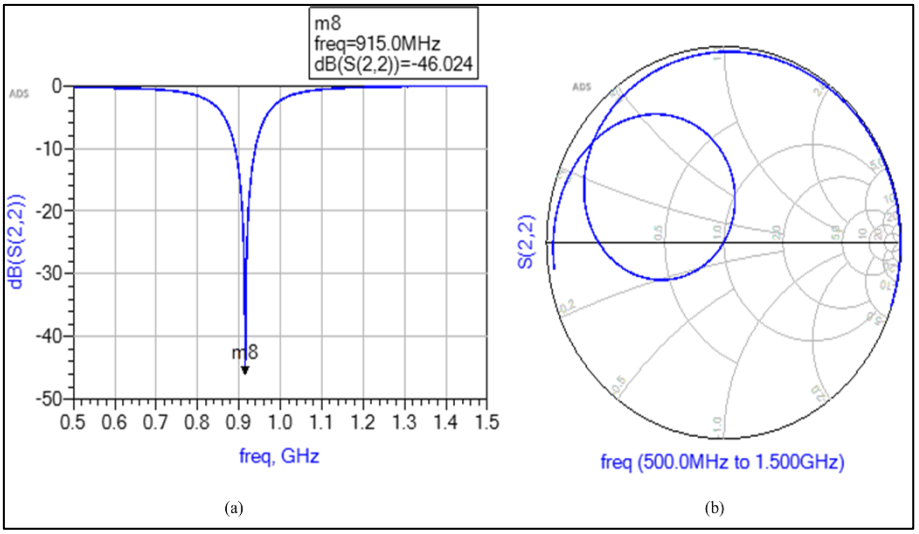


Figure 4.71. The $S_{(1,1)}$ for the six stages of DVM with T matching impedance.

Figure 4.71(a). shows the $S_{(1,1)}$ for six stages of DVM with T matching impedance and the result of about -46.024 dB. Figure 4.71(b) shows the Smith chart of the T matching impedance for 915 MHz that applied from 500 to 1500 MHz.

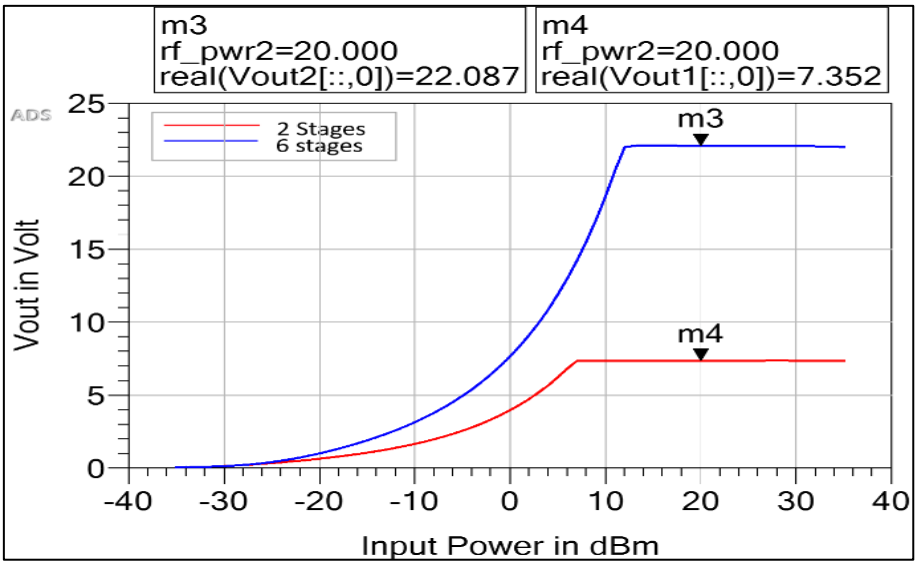


Figure 4.72. The V_{out} of DVM with and without T matching impedance from 20 KΩ to 2KΩ

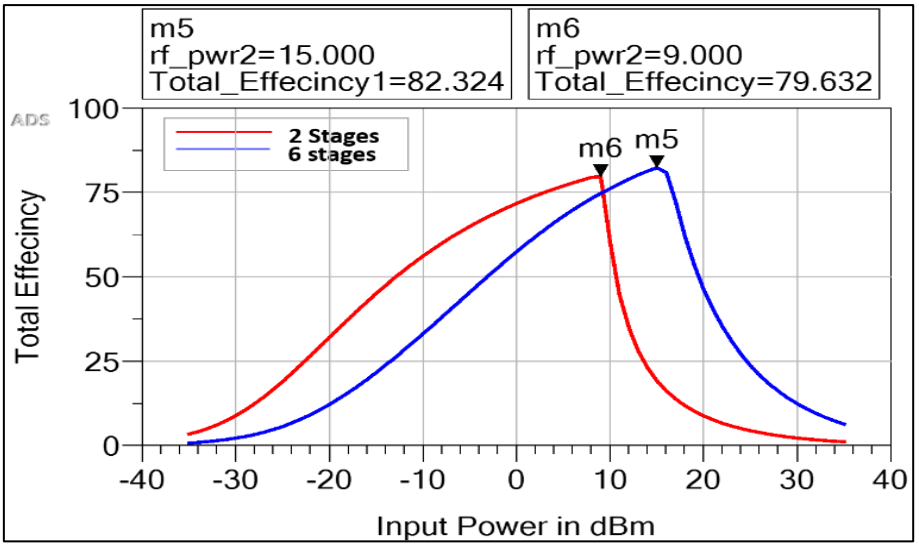


Figure 4. 73. The efficiency of DVM with and without T matching impedance from 25 to 50 KΩs of load conditions

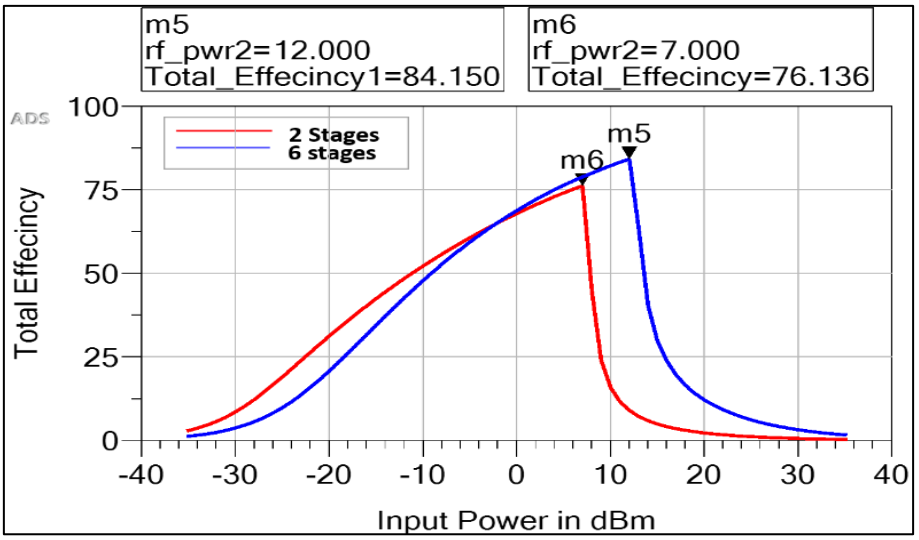


Figure 4.74. The efficiency of DVM with and without T matching impedance from 50 to 100 KΩs of load conditions

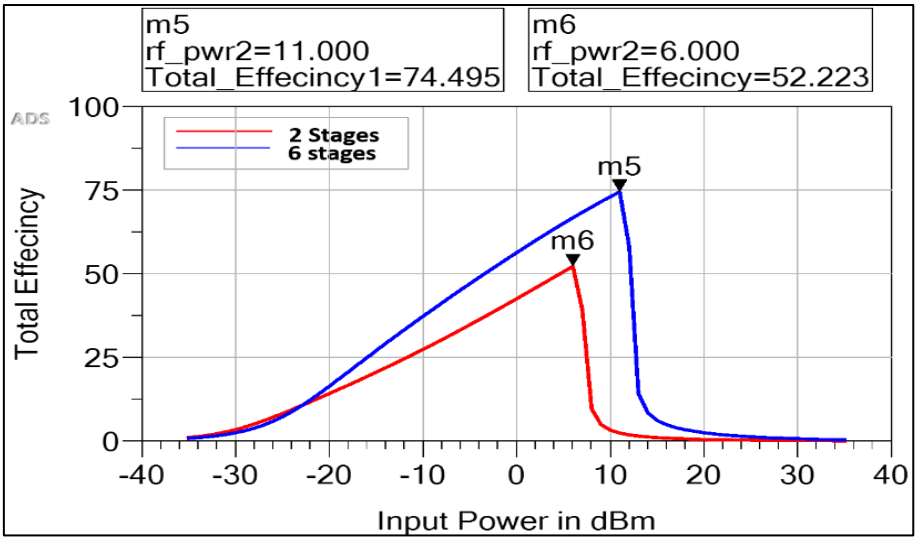


Figure 4.75. The efficiency of DVM with and without T matching impedance from100 to 500 KΩs of load conditions

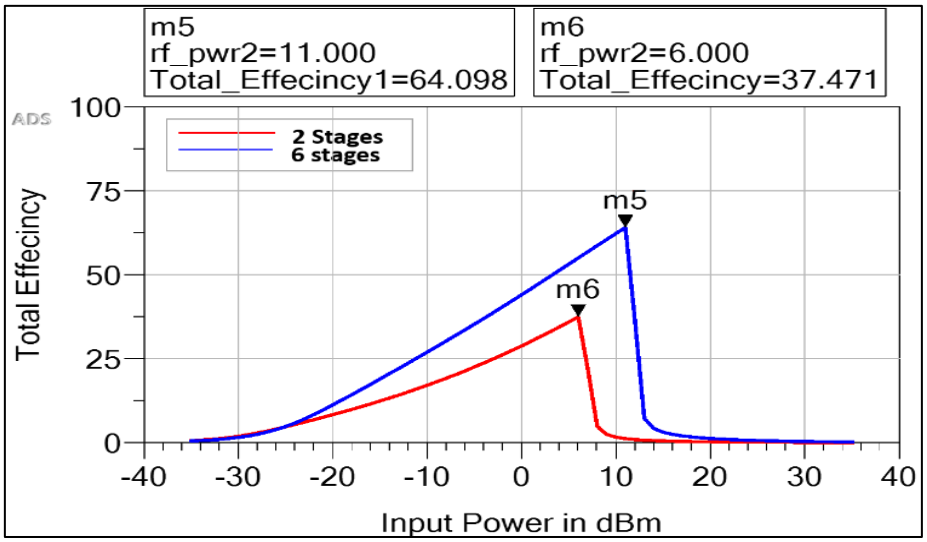


Figure 4.76. The efficiency of DVM with and without T matching impedance from 500 to 1000 KΩs of load conditions.

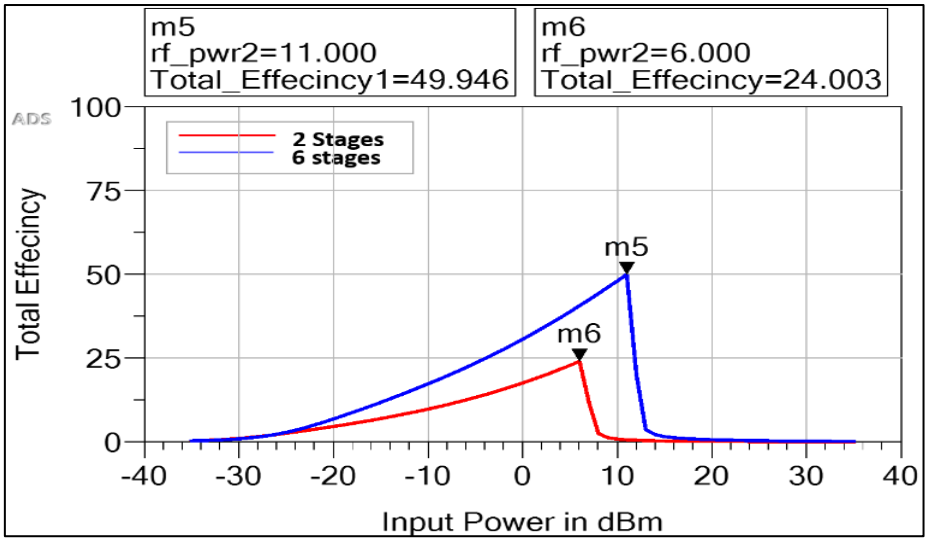


Figure 4.77. The efficiency of DVM with and without T matching impedance from 1000 to 2000 KΩs of load conditions

The simulation has been applied in the same ways with different load conditions for two and six stages with HSMS 2850 and T matching network. Therefore, according to Figure 4.72, which shows the Vout of the DVMs, that voltage is a table with the change of the load changes, and the value of voltage is affected by the number of stages, and the value increases with the increase in the number of stages of the DVM. On the other hand, increasing the number of stages directly affects the value of the matching impedance, which must be considered when designing to reach an equivalent circuit.

The same applies to the value of the efficiency of the circuit, as shown in Figure 4.73, Figure 4.74, Figure 4.75, Figure 4.76, and Figure 4.77, as it is affected by the number of stages in the circuit and also by the change in the value of the load resistance applied to the circuit.

4.3.2. The DVM Design With π Matching

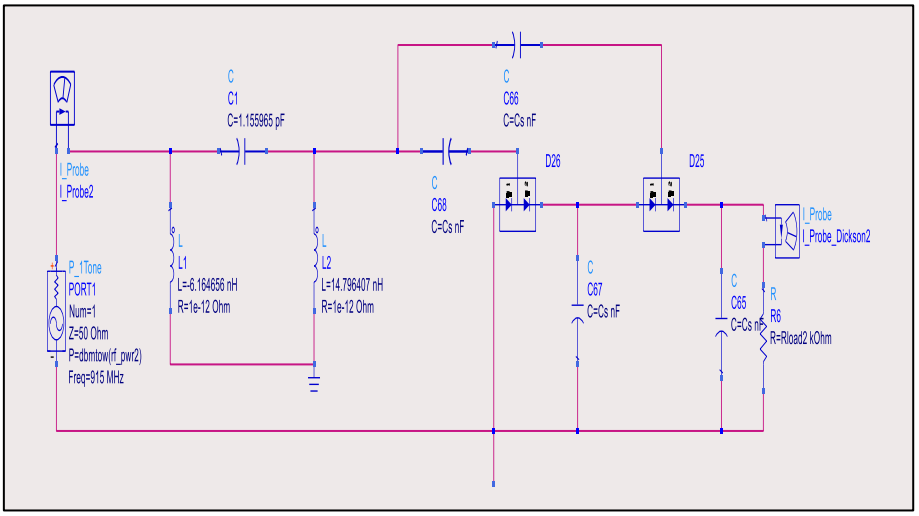


Figure 4.78. The two stages of the DVM circuit with π matching impedance

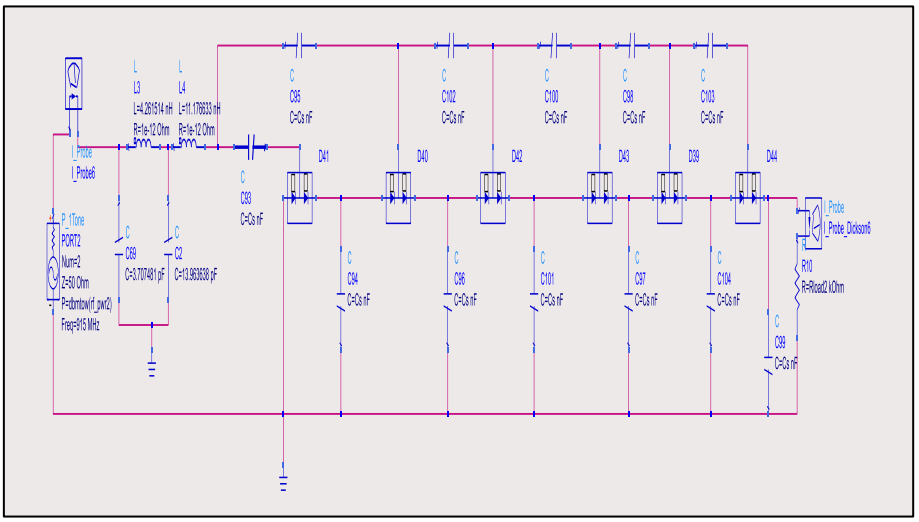


Figure 4.79. The six stages of the DVM circuit with π matching impedance

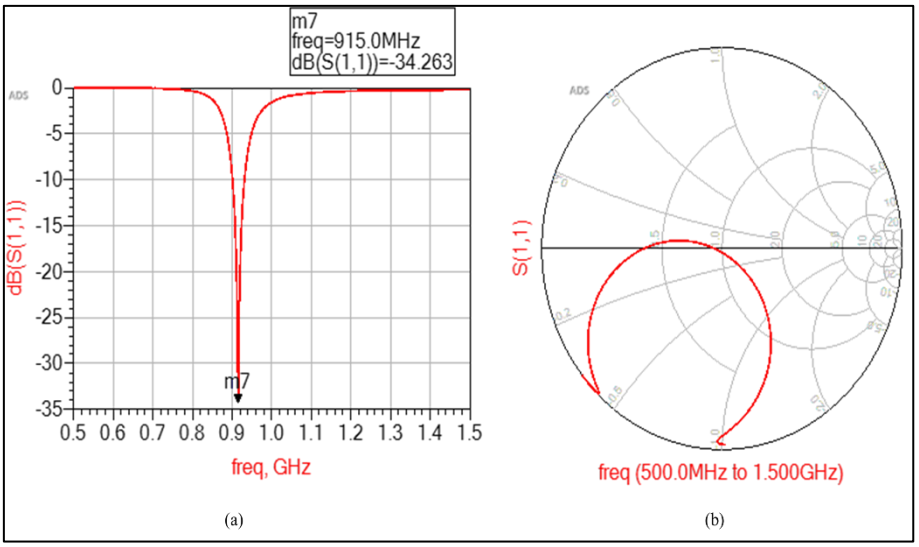


Figure 4.80. The $S_{(1,1)}$ for the two stages of DVM with L matching impedance.

Figure 4.80(a). shows the $S_{(1,1)}$ for two stages of DVM with π matching impedance and the result of about -34.263 dB. Figure 4.80(b) shows the Smith chart of the π matching impedance for 915 MHz that applied from 500 to 1500 MHz.

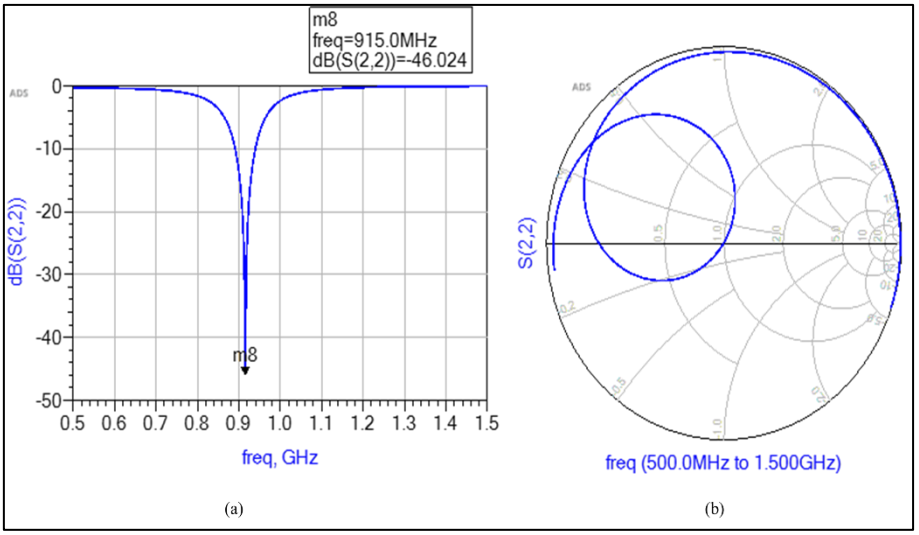


Figure 4.81. The $S_{(1,1)}$ for the six stages of DVM with π matching impedance.

Figure 4.81(a). shows the $S_{(1,1)}$ for two stages of DVM with π matching impedance and the result of about -46.024 dB. Figure 4.81(b) shows the Smith chart of the π matching impedance for 915 MHz that applied from 500 to 1500 MHz.

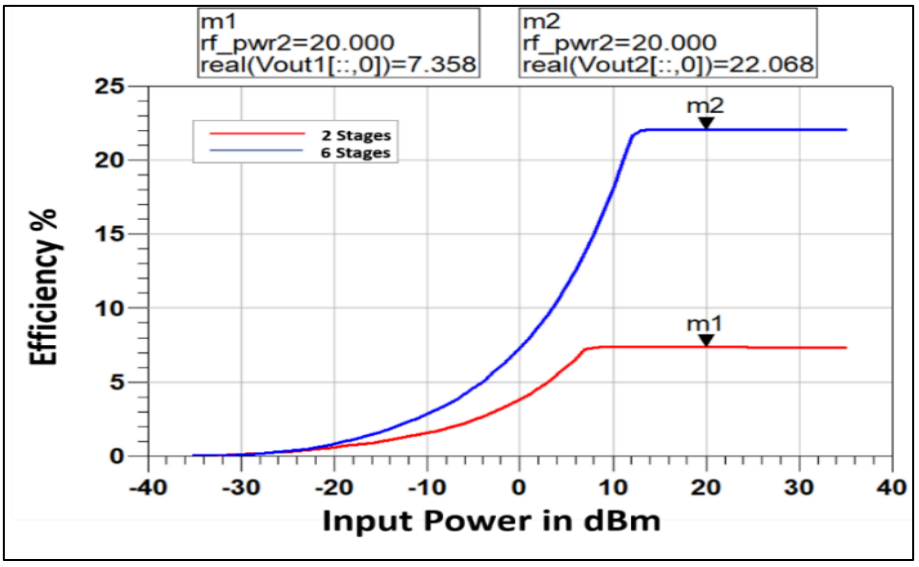


Figure 4.82. The output voltage of DVM stages with π matching from 20KΩ to 2000 KΩ

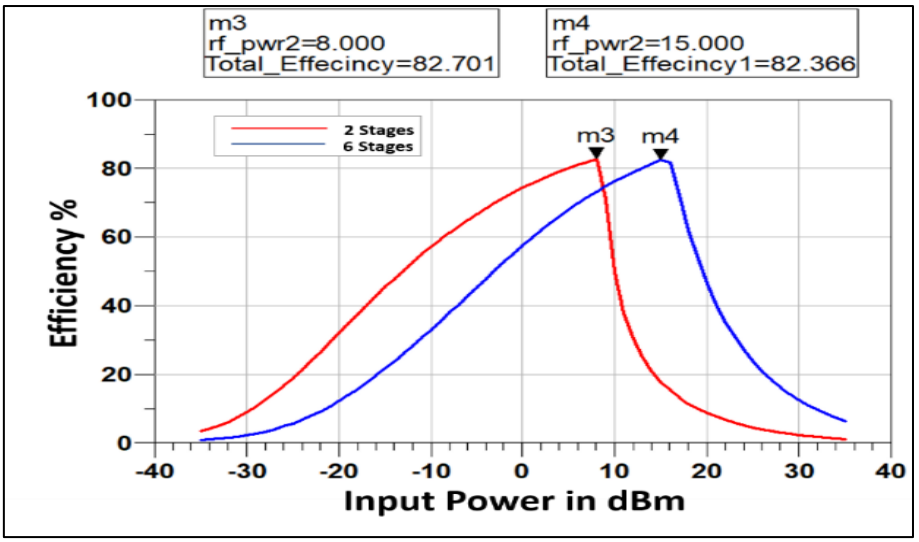


Figure 4.83. The efficiency of DVM with and without π matching impedance from 25 to 50 KΩs of load conditions

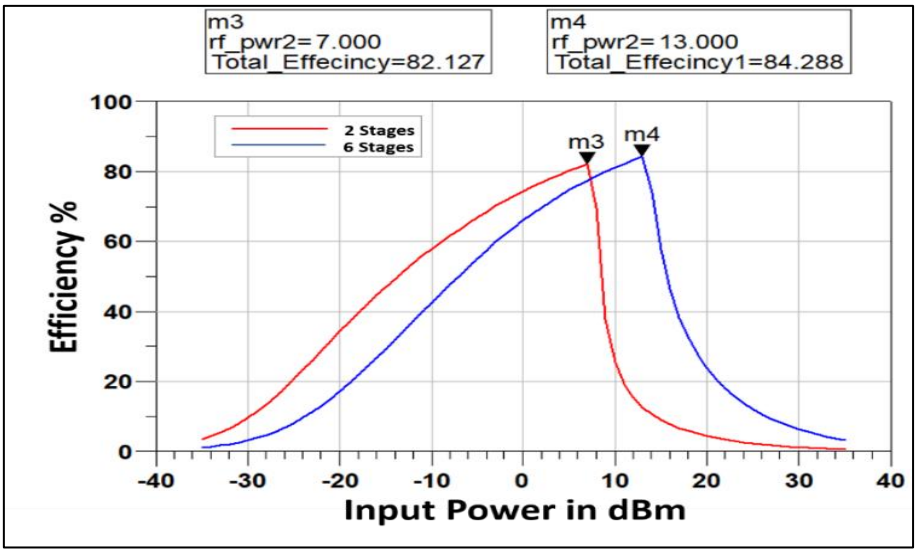


Figure 4.84. The efficiency of DVM with and without π matching impedance from 50 to 100 KΩs of load conditions

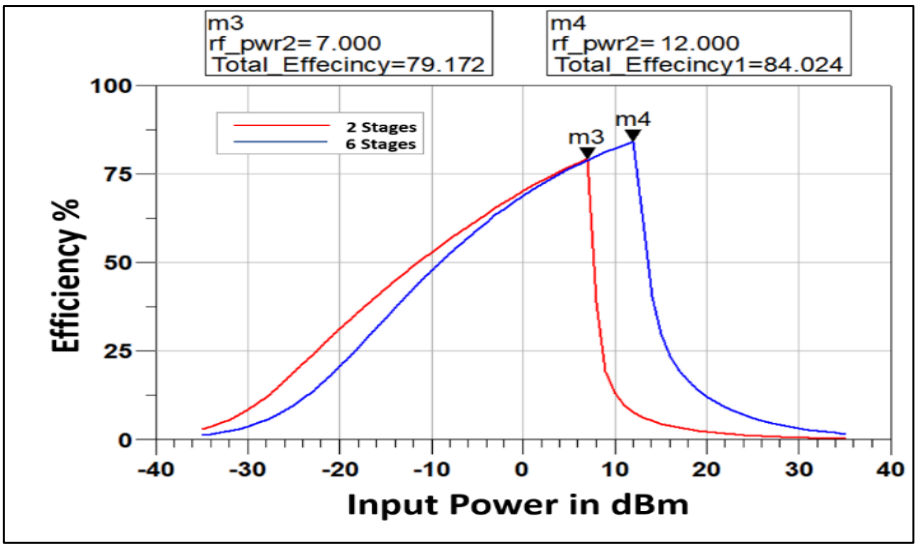


Figure 4.85. The efficiency of DVM with and without π matching impedance from100 to 500 KΩ of load conditions

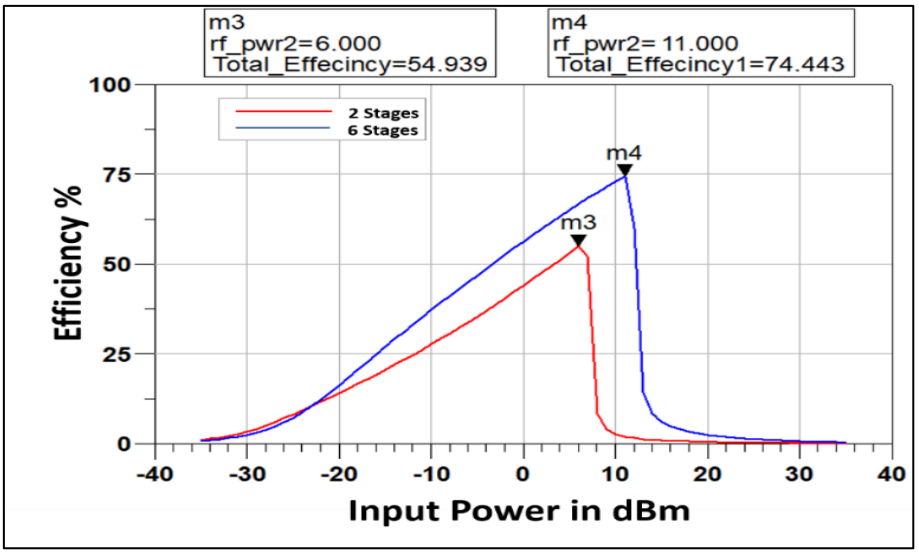


Figure 4.86. The efficiency of DVM with and without π matching impedance from100 to 500 KΩ of load conditions

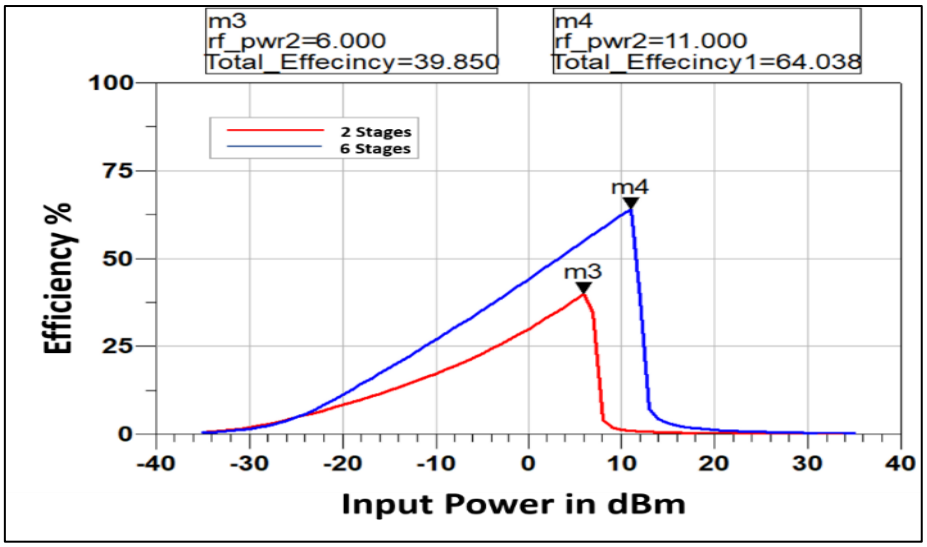


Figure 4.87. The efficiency 0 of DVM with and without π matching impedance 1000 to 2000 KΩ of load conditions

Figure 4.82 shows a diagram of the voltage outputs applied to the DVM cases. Besides Figure 4.823, figure 4.84, figure 4.85, figure 4.86, and Figure 4.87. The results explain that the voltage outputs depend on the number of DVM stages. Besides, the DVM stages affect the voltage and efficiency values, as shown in the circuit simulation results.

4.3.3. The Harvesting Circuit For HSMS 2860 Diode

In this section, DVM circuits are designed in one window Advanced Design System (ADS) using HSMS 2860 diodes. The design includes different amplifier stages, starting from two to six stages, as shown below. It will also analyze and examine each of the values of voltages and circuit equivalents and the effect of changing the stages on the value of Results

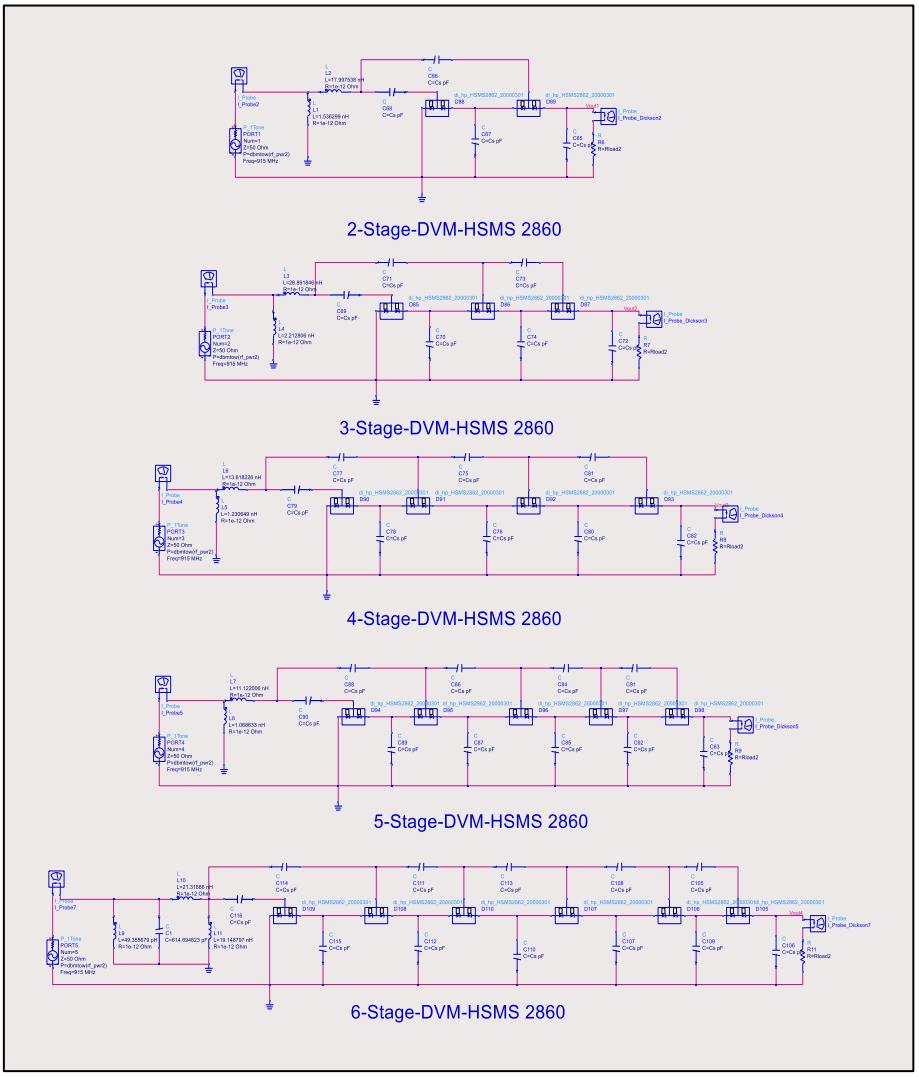


Figure 4.88. The stages of DVM circuits with L matching impedance and using HSMS 2862 Diode

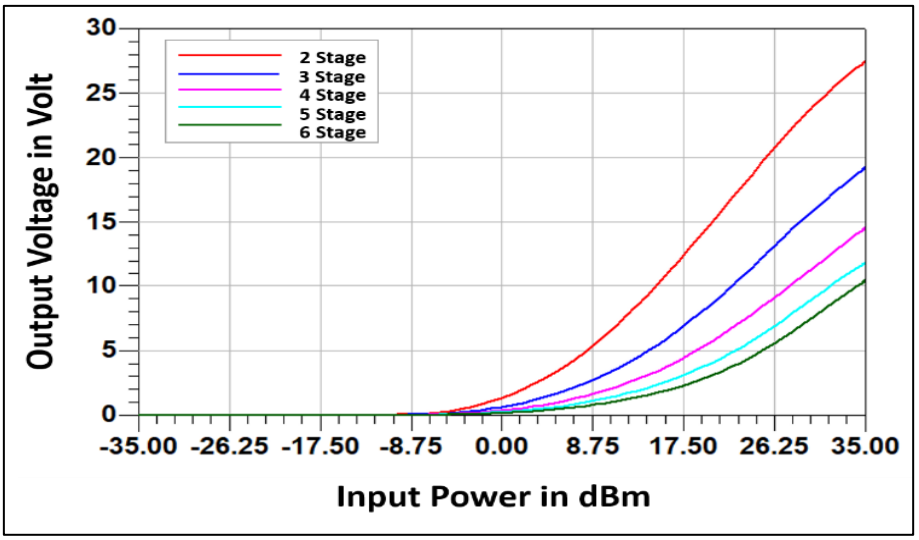


Figure 4.89. The V_{out} of DVM stages using L matching impedance for HSMS 2860 diode by applying 25 to 50 KΩ of load condition.

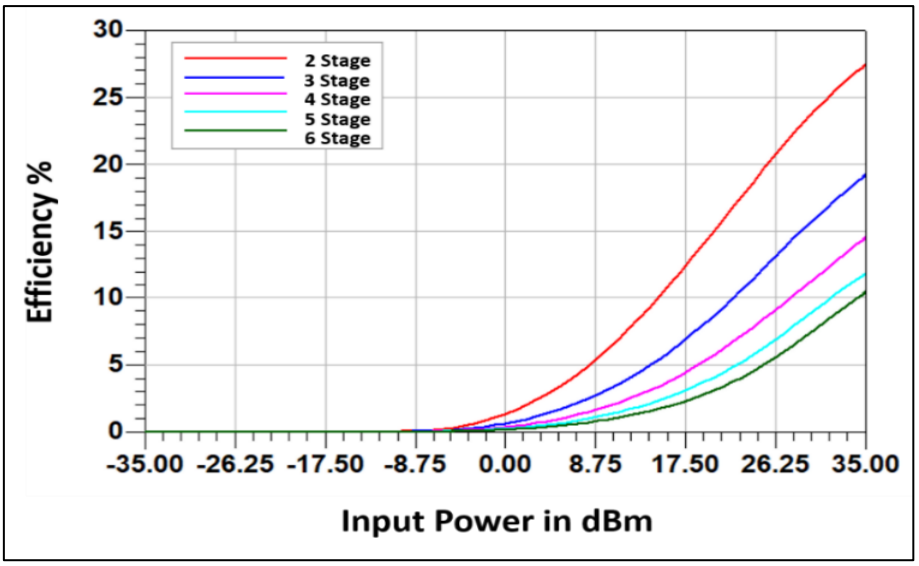


Figure 4.90. The efficiency of DVM stages using L matching impedance for HSMS 2860 diode by applying 25 to 50 KΩ of load condition

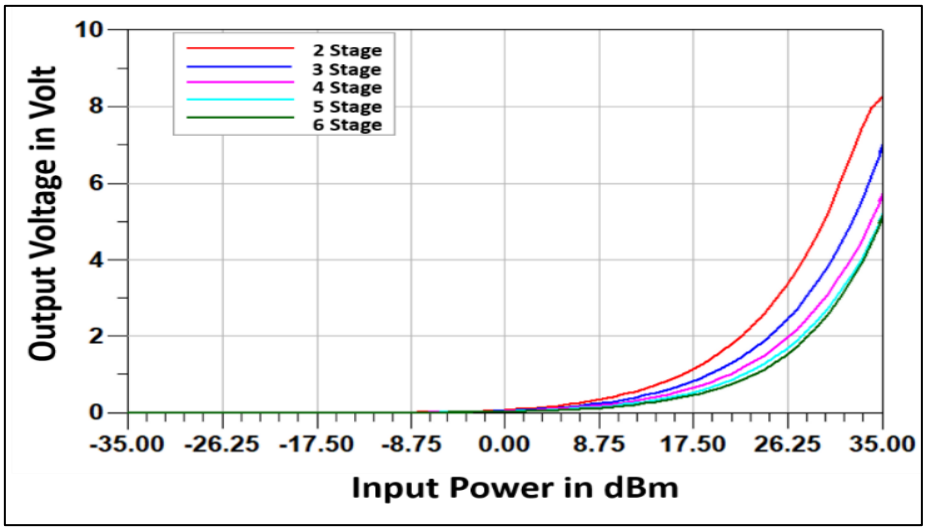


Figure 4.91. The V_{out} of DVM stages using L matching impedance for HSMS 2860 diode by applying 50 to 100 KΩ of load condition

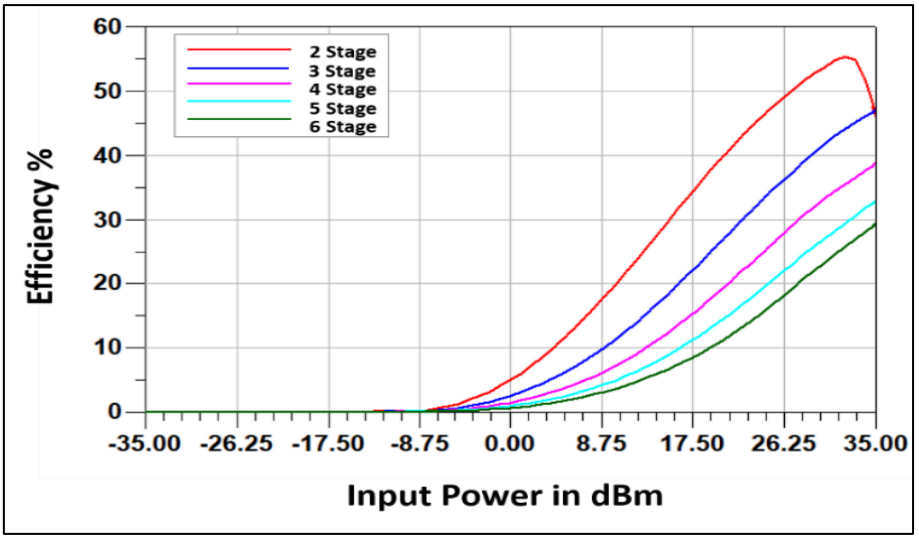


Figure 4.92. The efficiency of DVM stages using L matching impedance for HSMS 2860 diode by applying 50 to 100 KΩ of load condition

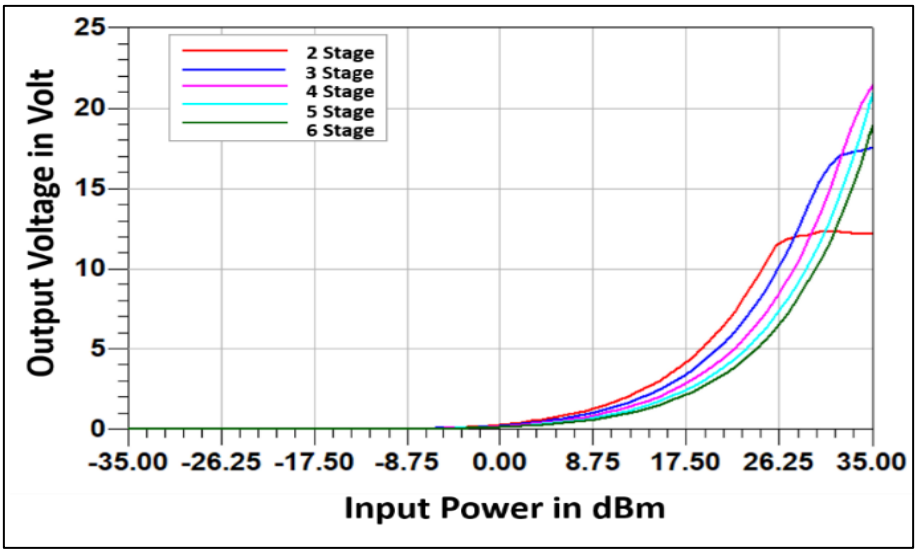


Figure 4.93. The V_{out} of DVM stages using L matching impedance for HSMS 2860 diode by applying 100 to 500 KΩ of load condition

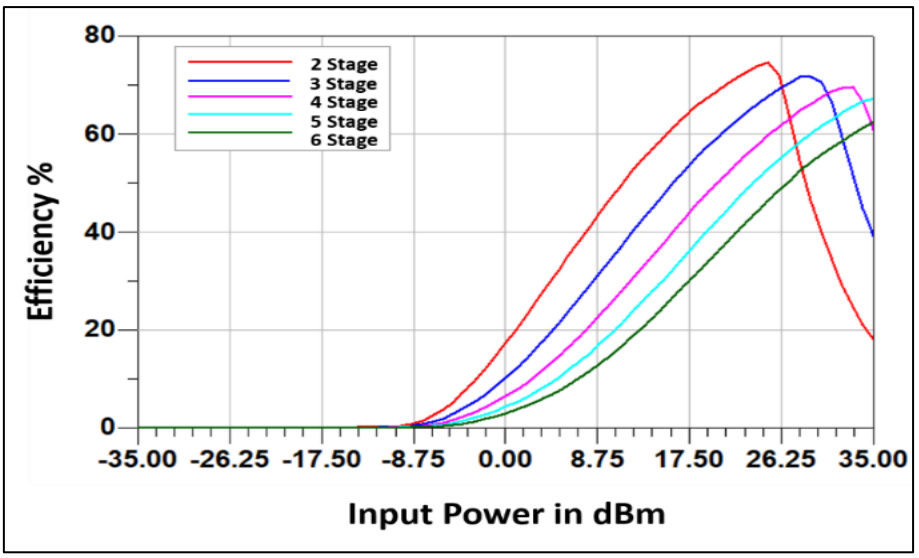


Figure 4.94. The efficiency of DVM stages using L matching impedance for HSMS 2860 diode by applying 100 to 500 KΩ of load condition

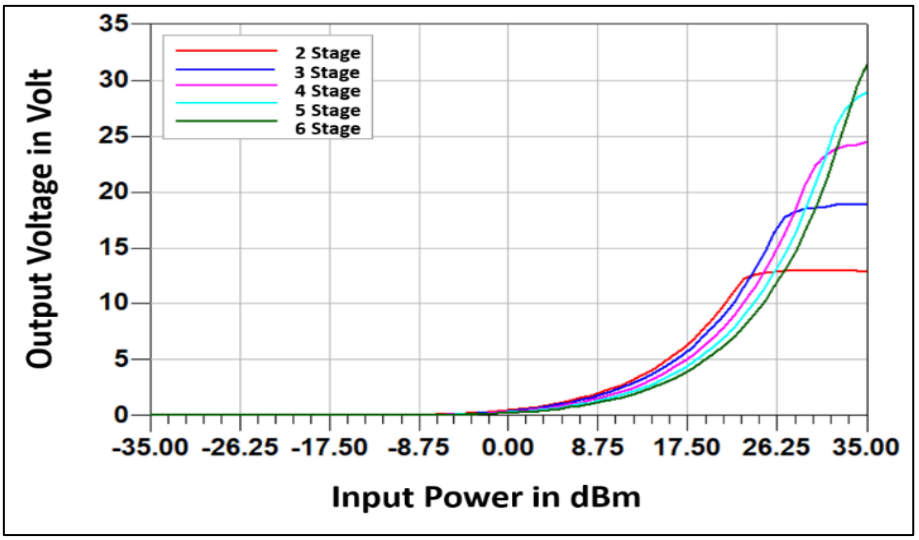


Figure 4.95. The efficiency of DVM stages using L matching impedance for HSMS 2860 diode by applied 500 to 1000 KΩ of load condition

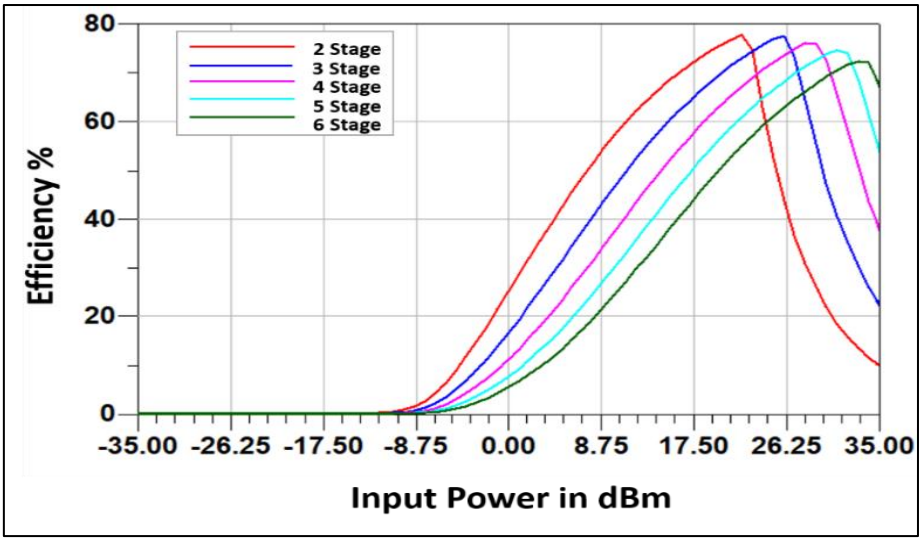


Figure 4.96. The efficiency of DVM stages using L matching impedance for HSMS 2860 diode by applying 500 to 1000 KΩ of load condition

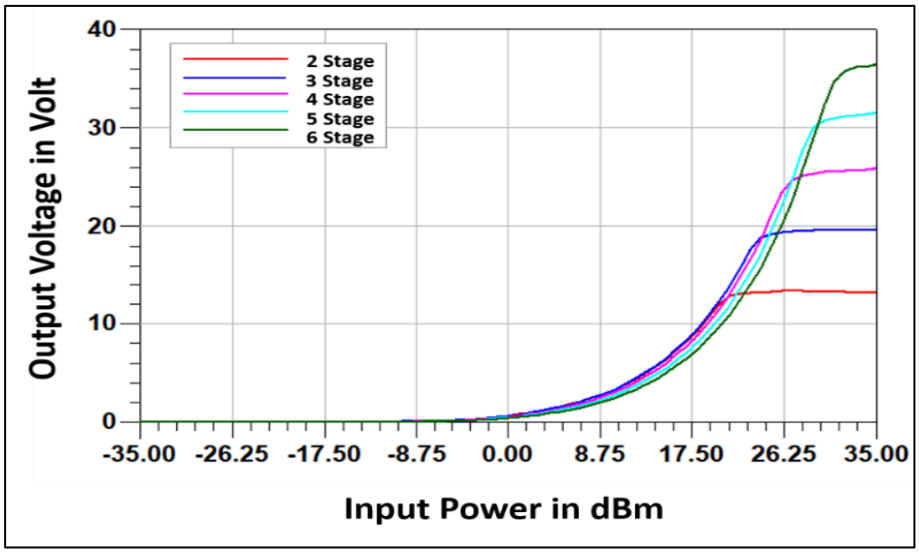


Figure 4.97. The efficiency of DVM stages using L matching impedance for HSMS 2860 diode by applying 1000 to 2000 KΩ of load conditions.

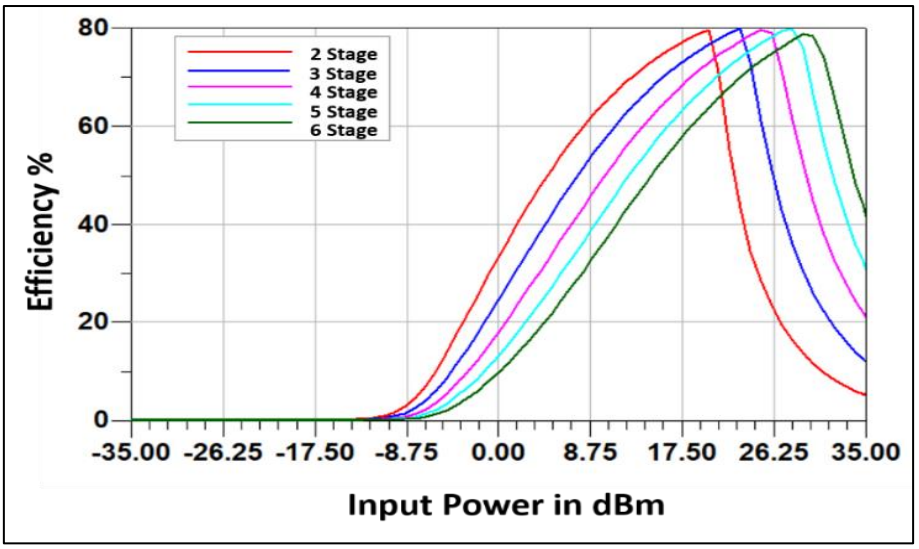


Figure 4.98. The efficiency of DVM stages using L matching impedance for HSMS 2860 diode applied 1000 to 2000 KΩ of load condition.

The simulation was done during the period of the input power at -35 to 35 dBm to test and simulate the voltage and the efficiency of the DVM stages. According to the result, Figures 4.88, figure 4.90, figure 4.92, figure 4.94, and figure 4.96 show the change in the voltage level while the change of DVM stages and the changes in the load conditions. Besides, Figures 4.89, figure 4.91, figure 4.93, figure 4.95, and figure 4.97 show the efficiency level during the same conditions. Hence, the result shows the effects of the number of stages on the voltage and efficiency of the rectifier.

4.4. THE SIMULATION RESULT OF THE QUALITY FACTOR

In this section of the thesis, the matching impedance circuit quality factor has been researched for various matching mechanism types and stages of DVM design using three different types of diode models, particularly the HSMS 2852, HSMS 2822, and HSMS 2860. The quality factor was applied to the DVM circuits of the variable load resistors. According to the results, the quality factor for L matching is represented in Table 4.1, and the quality factor of T matching is represented in Table 4.2. the result of π is shown in Table 4.3.

Table 4.1 The L matching quality factor results.

DVM stages	HSMS 2852 Circuit	HSMS 2822 Circuit	HSMS 2860 Circuit
Two-stages	5.8	6.3	6.4
Three stages	6	5.5	6.1
Four stages	4.5	5	5.2
Five stages	3.8	4.4	4
Six stages	3.5	4	3.8

Table 4.2. The T matching quality factor results.

DVM stages	HSMS 2852 Circuit	HSMS 2822 Circuit
Two stages	2.5	7.4
Six stages	3.7	7.5

Table 4.3. The π matching quality factor results.

DVM stages	HSMS 2852 Circuit	HSMS 2822 Circuit
Two stages	6.6	7.6
Six stages	4.5	8.3

As illustrated in Tables 4.1, 4.2, and 4.3, various quality results and values have been investigated according to applied various matching pattern types with different types and conditions of the DVM stage. There is a relationship between the value of the results of the quality coefficient and the impedance value of the circuit designed for the rectifier. That is, a small value of the output quality factor will result in the

corresponding response bandwidth of the designed impedance circuit. Also, the best results are when the value of the face factor is high or at its maximum. The last case can be used for harvesting radio wave applications.

PART 5

CONCLUSIONS

The Dickson voltage multiplier is a popular circuit topology that generates high DC voltages from a low input voltage. The circuit consists of a series of diode-capacitor stages interconnected in a ladder-like fashion, with each stage providing an incremental increase in voltage. The number of stages in a Dickson voltage multiplier directly impacts the output voltage and efficiency of the circuit. As the number of stages increases, the output voltage increases linearly, but the efficiency of the circuit decreases due to the increasing losses in the diodes and capacitors.

The efficiency of a Dickson voltage multiplier is affected by several factors, including the capacitance of the capacitors, the forward voltage drops of the diodes, and the switching frequency of the circuit. A higher capacitance will result in a higher output voltage, but it will also increase the charging time of the capacitors, which can decrease the overall efficiency of the circuit. Similarly, a lower forward voltage drop of the diodes will increase the efficiency of the circuit, but it may also limit the maximum output voltage that can be achieved.

The DVM's stage count can also impact the output ripple voltage of the circuit. Due to the capacitors' filtering action, the ripple voltage lowers as the number of stages rises. The circuit's load current can supply may be constrained by a high output impedance, which can also cause a high stage count. The result indicates that when the DVM stages increase, a harvesting circuit's output voltage will likewise grow. As demonstrated in the preceding chapter, the output voltage does not impact the matching circuit.

The Schottky diodes are an excellent choice for use in voltage multipliers due to their low forward voltage drop and fast switching times.

Among the three models you mentioned, the HSMS-2860 has the lowest forward voltage drop, which means it will have the highest efficiency in a voltage multiplier circuit. However, it is important to note that the choice of the diode is just one factor that can affect the efficiency of a voltage multiplier. The design of the multiplier circuit itself, as well as the input and output voltages and currents, will also play a role in determining the overall efficiency.

To provide a more specific comparison, we can look at some of the key electrical characteristics of each diode model:

- HSMS-2822: This diode has a maximum forward voltage drop of 0.4V at a forward current of 1mA and a maximum reverse voltage of 15V. Its typical capacitance is 0.7pF.
- HSMS-2850: This diode has a maximum forward voltage drop of 0.35V at a forward current of 1mA and a maximum reverse voltage of 20V. Its typical capacitance is 0.6pF.
- HSMS-2860: This diode has a maximum forward voltage drop of 0.28V at a forward current of 1mA and a maximum reverse voltage of 20V. Its typical capacitance is 0.6pF.

Based on these specifications, we can see that the HSMS-2860 has the lowest forward voltage drop and the highest reverse voltage rating, which makes it the most efficient choice for a Dickson voltage multiplier. However, the HSMS-2850 is also a good choice due to its low forward voltage drop and slightly higher reverse voltage rating compared to the HSMS-2822. Ultimately, the best choice of the diode will depend on the specific requirements of the designed voltage multiplier circuit.

In a Dickson voltage multiplier circuit, the diode-capacitor stages require a matching network to provide the necessary impedance matching between the input and output of the circuit. The most common matching networks are L-match, T-match, and π-match networks.

The choice of the matching network can significantly impact the output voltage and efficiency of the circuit. Generally, the L-match network is the most straightforward and widely used matching network for Dickson voltage multipliers. It consists of a series inductor and a shunt capacitor, providing the circuit impedance transformation. The L-match network is most effective at low frequencies and for circuits with a low number of stages.

- The T-match network is a more complex matching network that provides better impedance matching than the L-match network. It consists of a series inductor followed by a shunt capacitor and another series inductor. The T-match network is most effective for higher frequencies and circuits with more stages.
- The π-match network is the most complex matching network and provides the best impedance matching of the three networks. It consists of a series inductor, two shunt capacitors, and another series inductor. The π-match network is most effective at higher frequencies and for circuits with a very high number of stages.

The choice of the matching network can affect the output voltage and efficiency of the Dickson voltage multiplier in several ways. The L-match network provides the most straightforward impedance matching and is often used for simpler circuits, but it may not be as efficient as the other two networks for circuits with a higher number of stages. The T-match network provides better impedance matching than the L-match network and is often used for circuits with higher stages or at higher frequencies. The PI-match network provides the best impedance matching, but it is the most complex and may not be necessary for most applications.

Overall, the choice of matching network should be carefully considered based on the specific requirements of the Dickson voltage multiplier circuit, including the number of stages, the frequency of operation, and the desired output voltage and efficiency. Proper selection and implementation of the matching network can significantly improve the performance of the circuit.

As a conclusion to this comparison, matching topology is also examined in this thesis for various stage numbers. First, a two-stage DVM with a 25 to 50 kΩ load resistance produced results that demonstrated L-matching and T-matching topologies to be superior to π matching network topologies. Additionally, there is no difference in efficiency at high input power between the circuits with and without matching. Moreover, using a six-stage DVM with a 25 to 50 k of load resistance demonstrated that the matching type did not impact the harvesting circuit's efficiency. When the number of stages is lower, the T and L matching network is superior to the π matching topology for the effect of matching topology.

The load resistance can affect the output voltage of the Dickson voltage multiplier circuit in several ways. Firstly, it affects how much current the circuit can deliver to the load. As the load resistance decreases, the amount of current that can be delivered to the load increases, which can decrease the output voltage due to increased voltage drops across the diodes and capacitors.

Secondly, the load resistance can affect the output impedance of the Dickson voltage multiplier circuit. A higher load resistance results in a higher output impedance, which can limit the amount of current that can be delivered to the load. This can decrease the output voltage due to increased voltage drops across the diodes and capacitors.

Thirdly, the load resistance can affect the output ripple voltage of the circuit. As the load resistance decreases, the output ripple voltage of the circuit can increase due to the increased capacitive coupling between the output and ground.

Finally, the load resistance can affect the efficiency of the DVM circuit. As the load resistance decreases, the efficiency of the circuit can decrease due to the increased voltage drops across the diodes and capacitors. This can result in a decrease in the output voltage and an increase in power dissipation in the circuit. The 915 MHz RF energy harvesting is particularly well-suited for low-power applications due to its ability to capture ambient radio frequency signals and convert them into usable electrical power. These low-power applications benefit from the convenience,

sustainability, and cost-effectiveness that RF energy harvesting offers. Here are some notable low-power applications where 915 MHz RF energy harvesting excels:

- Wireless Sensors: Low-power wireless sensors used in environmental monitoring, agriculture, industrial automation, and smart buildings can benefit from RF energy harvesting at 915 MHz. These sensors can operate autonomously without the need for frequent battery replacements or external power sources, making them ideal for remote and hard-to-reach locations.
- Wearable Devices: Wearable technology, such as smartwatches, fitness trackers, and medical devices, often require low power to extend battery life. RF energy harvesting at 915 MHz can be integrated into these wearables, allowing them to recharge from ambient RF signals, reducing the need for constant recharging and enhancing user convenience.
- RFID Tags: Radio-Frequency Identification (RFID) tags used for asset tracking, inventory management, and logistics can be powered by 915 MHz RF energy harvesting. These low-power RFID tags can offer an efficient and cost-effective way to track and manage assets without the need for traditional batteries.
- Smart Labels and Packaging: In retail and supply chain management, low-power smart labels and packaging can provide real-time tracking and monitoring of products. RF energy harvesting at 915 MHz enables these smart labels to harvest energy from their surroundings, eliminating the need for frequent battery replacements.
- Energy-Efficient Wireless Communication Devices: Low-power wireless communication devices, such as short-range transceivers used in home automation and IoT applications, can be powered by 915 MHz RF energy harvesting. This energy-efficient approach reduces the overall power consumption of these devices.
- Energy Harvesting Switches: Low-power wireless switches that control lighting, appliances, or other devices can utilize RF energy harvesting at 915 MHz. These switches can be self-powered and easily installed without the need for wiring or batteries.

- Remote Monitoring Systems: Remote monitoring systems, like weather stations or wildlife trackers, often operate in isolated areas where access to power is limited. RF energy harvesting at 915 MHz enables these systems to operate for extended periods without human intervention.
- Environmental and Structural Monitoring: Low-power sensors used for environmental and structural monitoring applications can benefit from 915 MHz RF energy harvesting. These sensors can provide real-time data on temperature, humidity, vibrations, and other parameters without the need for frequent maintenance.

In all these low-power applications, 915 MHz RF energy harvesting offers a viable and sustainable power source, reducing the environmental impact and maintenance costs associated with conventional power solutions. As technology continues to advance, RF energy harvesting is expected to play an even more significant role in powering an ever-growing range of low-power devices and systems.

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APPENDIX LIST

Appendeix A: The datasheet of AVAGO HSMS-282x Surface Mount RF Schottky Barrier Diodes

Appendeix B: The datasheet of AVAGO HSMS-285x Surface Mount RF Schottky Barrier Diodes

Appendeix C: The datasheet of AVAGO HSMS-286x Surface Mount RF Schottky Barrier Diodes

APPENDEIX A

HSMS-282x

Surface Mount RF Schottky Barrier Diodes

AVAGO TECHNOLOGIES

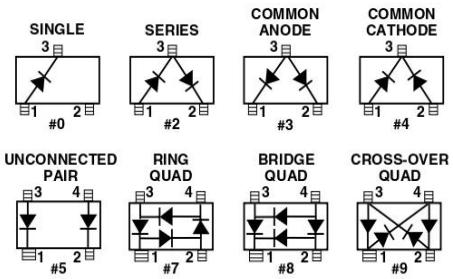
Data Sheet

Description/Applications

These Schottky diodes are specifically designed for both analog and digital applications. This series offers a wide range of specifications and package configurations to give the designer wide flexibility. Typical applications of these Schottky diodes are mixing, detecting, switching, sampling, clamping, and wave shaping. The HSMS-282x series of diodes is the best all-around choice for most applications, featuring low series resistance, low forward voltage at all current levels and good RF characteristics.

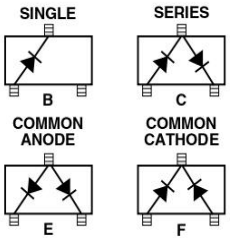
Note that Avago's manufacturing techniques assure that dice found in pairs and quads are taken from adjacent sites on the wafer, assuring the highest degree of match.

Package Lead Code Identification, SOT-23/SOT-143 (Top View)



Package Lead Code Identification, SOT-323

(Top View)

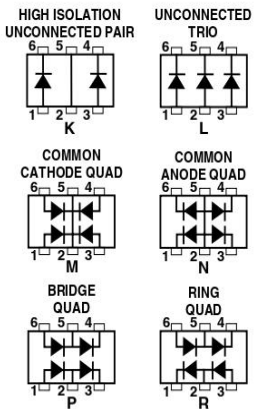


Features

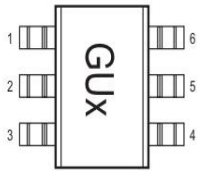
- Low Turn-On Voltage (As Low as 0.34 V at 1 mA)
- Low FIT (Failure in Time) Rate*
- Six-sigma Quality Level
- Single, Dual and Quad Versions
- Unique Configurations in Surface Mount SOT-363 Package
  - increase flexibility
  - save board space
  - reduce cost
- HSMS-282K Grounded Center Leads Provide up to 10 dB Higher Isolation
- Matched Diodes for Consistent Performance
- Better Thermal Conductivity for Higher Power Dissipation
- Lead-free Option Available
- For more information see the Surface Mount Schottky Reliability Data Sheet.

Package Lead Code Identification, SOT-363

(Top View)



Pin Connections and Package Marking



Notes:
1. Package marking provides orientation and identification.
2. See "Electrical Specifications" for appropriate package marking.

Absolute Maximum Ratings[1] $T_C = 25°C$

Symbol	Parameter	Unit	SOT-23/SOT-143	SOT-323/SOT-363
I_f	Forward Current (1 µs Pulse)	Amp	1	1
P_{IV}	Peak Inverse Voltage	V	15	15
T_j	Junction Temperature	°C	150	150
T_{stg}	Storage Temperature	°C	-65 to 150	-65 to 150
θ_{jc}	Thermal Resistance[2]	°C/W	500	150

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to the device.
2. $T_C = +25°C$, where T_C is defined to be the temperature at the package pins where contact is made to the circuit board.

Electrical Specifications $T_C = 25°C$, Single Diode[3]

Part Number HSMS[4]	Package Marking Code	Lead Code	Configuration	Minimum Breakdown Voltage V_{BR} (V)	Maximum Forward Voltage V_F (mV)	Maximum Forward Voltage V_F (V) @ I_F (mA)	Maximum Reverse Leakage I_R (nA) @ V_R (V)	Maximum Capacitance C_T (pF)	Typical Dynamic Resistance R_D (Ω)[5]
2820	C0	0	Single	15	340	0.5 10	100 1	1.0	12
2822	C2	2	Series						
2823	C3	3	Common Anode						
2824	C4	4	Common Cathode						
2825	C5	5	Unconnected Pair						
2827	C7	7	Ring Quad[4]						
2828	C8	8	Bridge Quad[4]						
2829	C9	9	Cross-over Quad						
282B	C0	B	Single						
282C	C2	C	Series						
282E	C3	E	Common Anode						
282F	C4	F	Common Cathode						
282K	CK	K	High Isolation Unconnected Pair						
282L	CL	L	Unconnected Trio						
282M	HH	M	Common Cathode Quad						
282N	NN	N	Common Anode Quad						
282P	CP	P	Bridge Quad						
282R	OO	R	Ring Quad						
Test Conditions				$I_R = 100$ µA	$I_F = 1$ mA[1]			$V_R = 0V$[2] f = 1 MHz	$I_F = 5$ mA

Notes:
1. ΔV_F for diodes in pairs and quads in 15 mV maximum at 1 mA.
2. ΔC_{TO} for diodes in pairs and quads is 0.2 pF maximum.
3. Effective Carrier Lifetime (τ) for all these diodes is 100 ps maximum measured with Krakauer method at 5 mA.
4. See section titled "Quad Capacitance."
5. $R_D = R_s + 5.2\Omega$ at 25°C and $I_f = 5$ mA.

Quad Capacitance

Capacitance of Schottky diode quads is measured using an HP4271 LCR meter. This instrument effectively isolates individual diode branches from the others, allowing accurate capacitance measurement of each branch or each diode. The conditions are: 20 mV R.M.S. voltage at 1 MHz. Avago defines this measurement as "CM", and it is equivalent to the capacitance of the diode by itself. The equivalent diagonal and adjacent capaci-tances can then be calculated by the formulas given below.

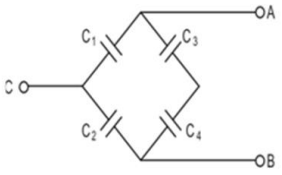
In a quad, the diagonal capacitance is the capacitance between points A and B as shown in the figure below. The diagonal capacitance is calculated using the following formula

$$C_{DIAGONAL} = \frac{C_1 \times C_2}{C_1 + C_2} + \frac{C_3 \times C_4}{C_3 + C_4}$$

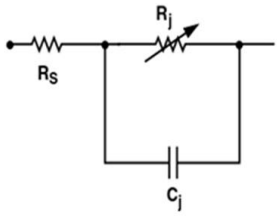
The equivalent adjacent capacitance is the capacitance between points A and C in the figure below. This capacitance is calculated using the following formula

$$C_{ADJACENT} = C_1 + \frac{1}{\frac{1}{C_2} + \frac{1}{C_3} + \frac{1}{C_4}}$$

This information does not apply to cross-over quad diodes.



Linear Equivalent Circuit Model Diode Chip



R_S = series resistance (see Table of SPICE parameters)

C_j = junction capacitance (see Table of SPICE parameters)

$$R_j = \frac{8.33 \times 10^{-5}\, nT}{I_b + I_s}$$

where

I_b = externally applied bias current in amps

I_s = saturation current (see table of SPICE parameters)

T = temperature, °K

n = ideality factor (see table of SPICE parameters)

Note:
To effectively model the packaged HSMS-282x product, please refer to Application Note AN1124.

ESD WARNING:
Handling Precautions Should Be Taken To Avoid Static Discharge.

SPICE Parameters

Parameter	Units	HSMS-282x
B_V	V	15
C_{J0}	pF	0.7
E_G	eV	0.69
I_{BV}	A	1E-4
I_S	A	2.2E-8
N		1.08
R_S	Ω	6.0
P_B	V	0.65
P_T		2
M		0.5

Typical Performance, T_C = 25°C (unless otherwise noted), Single Diode

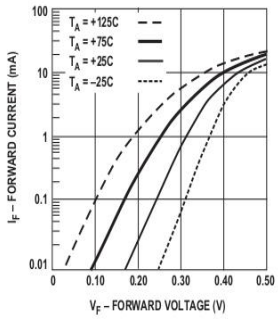


Figure 1. Forward Current vs. Forward Voltage at Temperatures.

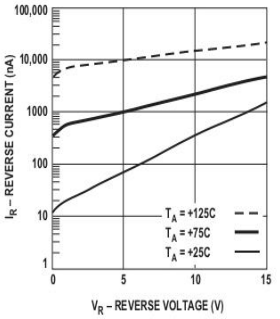


Figure 2. Reverse Current vs. Reverse Voltage at Temperatures.

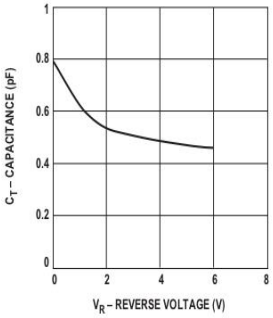


Figure 3. Total Capacitance vs. Reverse Voltage.

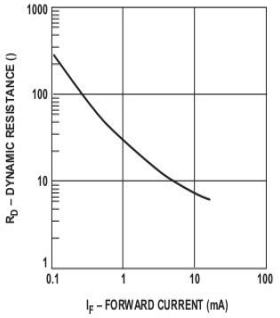


Figure 4. Dynamic Resistance vs. Forward Current.

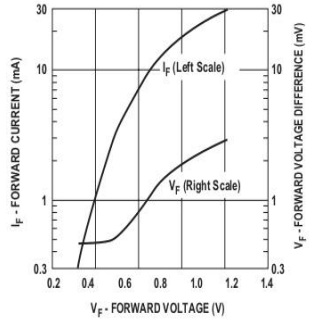


Figure 5. Typical V_f Match, Series Pairs and Quads at Mixer Bias Levels.

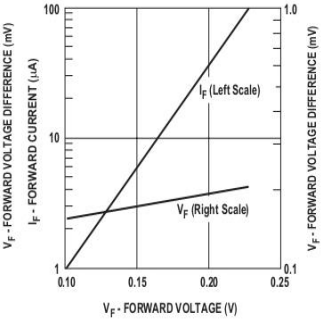


Figure 6. Typical V_f Match, Series Pairs at Detector Bias Levels.

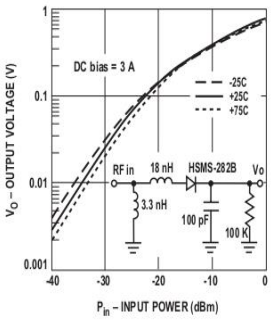


Figure 7. Typical Output Voltage vs. Input Power, Small Signal Detector Operating at 850 MHz.

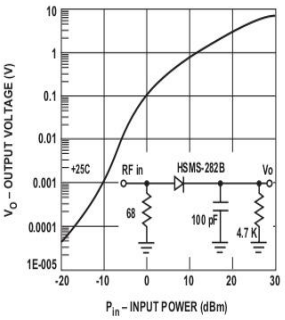


Figure 8. Typical Output Voltage vs. Input Power, Large Signal Detector Operating at 915 MHz.

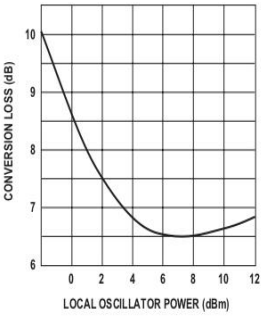


Figure 9. Typical Conversion Loss vs. L.O. Drive, 2.0 GHz (Ref AN997).

Applications Information

Product Selection

Avago's family of surface mount Schottky diodes provide unique solutions to many design problems. Each is optimized for certain applications.

The first step in choosing the right product is to select the diode type. All of the products in the HSMS-282x family use the same diode chip–they differ only in package configuration. The same is true of the HSMS-280x, -281x, 285x, -286x and -270x families. Each family has a different set of characteristics, which can be compared most easily by consulting the SPICE parameters given on each data sheet.

The HSMS-282x family has been optimized for use in RF applications, such as

- DC biased small signal detectors to 1.5 GHz.
- Biased or unbiased large signal detectors (AGC or power monitors) to 4 GHz.
- Mixers and frequencymultipliers to 6 GHz.

The other feature of the HSMS-282x family is its unit-to-unit and lot-to-lot consistency. The silicon chip used in this series has been designed to use the fewest possible processing steps to minimize variations in diode characteristics. Statistical data on the consistency of this product, in terms of SPICE parameters, is available from Avago.

For those applications requiring very high breakdown voltage, use the HSMS-280x family of diodes. Turn to the HSMS-281x when you need very low flicker noise. The HSMS-285x is a family of zero bias detector diodes for small signal applications. For high frequency detector or mixer applications, use the HSMS-286x family. The HSMS-270x is a series of specialty diodes for ultra high speed clipping and clamping in digital circuits.

Schottky Barrier Diode Characteristics

Stripped of its package, a Schottky barrier diode chip consists of a metal-semiconductor barrier formed by deposition of a metal layer on a semiconductor. The most common of several different types, the passivated diode, is shown in Figure 10, along with its equivalent circuit.

R_S is the parasitic series resistance of the diode, the sum of the bondwire and leadframe resistance, the resistance of the bulk layer of silicon, etc. RF energy coupled into R_S is lost as heat—it does not contribute to the rectified output of the diode. C_j is parasitic junction capacitance of the diode, controlled by the thick-ness of the epitaxial layer and the diameter of the Schottky contact. R_j is the junction resistance of the diode, a function of the total current flowing through it.

$$R_j = \frac{8.33 \times 10^{-5} nT}{I_S + I_b} = R_V - R_S$$

$$\approx \frac{0.026}{I_S + I_b} \text{ at } 25\,^{\circ}C$$

where

n = ideality factor (see table of SPICE parameters)

T = temperature in °K

I_S = saturation current (see table of SPICE parameters)

I_b = externally applied bias current in amps

R_v = sum of junction and series resistance, the slope of the V-I curve

I_S is a function of diode barrier height, and can range from picoamps for high barrier diodes to as much as 5 µA for very low barrier diodes.

The Height of the Schottky Barrier

The current-voltage characteristic of a Schottky barrier diode at room temperature is described by the following equation:

$$I = I_S \left(e^{\frac{V - IR_S}{0.026}} - 1\right)$$

On a semi-log plot (as shown in the Avago catalog) the current graph will be a straight line with inverse slope 2.3 X 0.026 = 0.060 volts per cycle (until the effect of R_S is seen in a curve that droops at high current). All Schottky diode curves have the same slope, but not necessarily the same value of current for a given voltage. This is determined by the saturation current, I_S, and is related to the barrier height of the diode.

Through the choice of p-type or n-type silicon, and the selection of metal, one can tailor the characteristics of a Schottky diode. Barrier height will be altered, and at the same time CJ and RS will be changed. In general, very low barrier height diodes (with high values of IS, suitable for zero bias applications) are realized on p-type silicon. Such diodes suffer from higher values of RS than do the n-type.

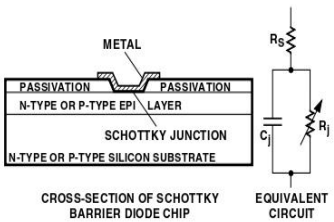


Figure 10. Schottky Diode Chip.

Thus, p-type diodes are generally reserved for detector applications (where very high values of RV swamp out high RS) and n-type diodes such as the HSMS-282x are used for mixer applications (where high L.O. drive levels keep RV low). DC biased detectors and self-biased detectors used in gain or power control circuits.

Detector Applications

Detector circuits can be divided into two types, large signal (P_{in} > -20 dBm) and small signal (P_{in} < -20 dBm). In general, the former use resistive impedance matching at the input to improve flatness over frequency — this is possible since the input signal levels are high enough to produce adequate output voltages without the need for a high Q reactive input matching network. These circuits are self-biased (no external DC bias) and are used for gain and power control of amplifiers.

Small signal detectors are used as very low cost receivers, and require a reactive input impedance matching network to achieve adequate sensitivity and output voltage. Those operating with zero bias utilize the HSMS- 285x family of detector diodes. However, superior performance over temperature can be achieved with the use of 3 to 30 µA of DC bias. Such circuits will use the HSMS-282x family of diodes if the operating frequency is 1.5 GHz or lower.

Typical performance of single diode detectors (using HSMS-2820 or HSMS-282B) can be seen in the transfer curves given in Figures 7 and 8. Such detectors can be realized either as series or shunt circuits, as shown in Figure 11.

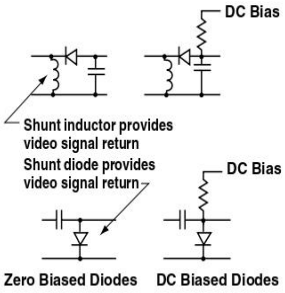


Figure 11. Single Diode Detectors.

The series and shunt circuits can be combined into a voltage doubler[1], as shown in Figure 12. The doubler offers three advantages over the single diode circuit.

- The two diodes are in parallel in the RF circuit, lowering the input impedance and making the design of the RF matching network easier.
- The two diodes are in series in the output (video) circuit, doubling the output voltage.
- Some cancellation of even-order harmonics takes place at the input.

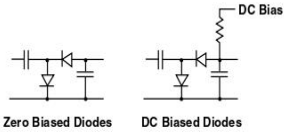


Figure 12. Voltage Doubler.

The most compact and lowest cost form of the doubler is achieved when the HSMS-2822 or HSMS-282C series pair is used.

Both the detection sensitivity and the DC forward voltage of a biased Schottky detector are temperature sensitive. Where both must be compensated over a wide range of temperatures, the differential detector[2] is often used. Such a circuit requires that the detector diode and the reference diode exhibit identical characteristics at all DC bias levels and at all temperatures. This is accomplished through the use of two diodes in one package, for example the HSMS-2825 in Figure 13. In the Avago assembly facility, the two dice in a surface mount package are taken from adjacent sites on the wafer (as illustrated in Figure 14). This assures that the characteristics of the two diodes are more highly matched than would be possible through individual testing and hand matching.

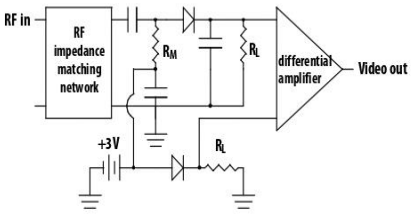


Figure 13. Differential Detector.

[1] Avago Application Note 956-4, "Schottky Diode Voltage Doubler."

[2] Raymond W. Waugh, "Designing Large-Signal Detectors for Handsets and Base Stations," Wireless Systems Design, Vol. 2, No. 7, July 1997, pp 42 – 48.

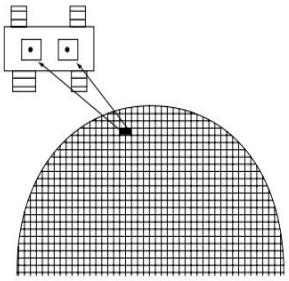


Figure 14. Fabrication of Avago Diode Pairs.

In high power applications, coupling of RF energy from the detector diode to the reference diode can introduce error in the differential detector. The HSMS-282K diode pair, in the six lead SOT-363 package, has a copper bar between the diodes that adds 10 dB of additional isolation between them. As this part is manufactured in the SOT-363 package it also provides the benefit of being 40% smaller than larger SOT-143 devices. The HSMS-282K is illustrated in Figure 15—note that the ground connections must be made as close to the package as possible to minimize stray inductance to ground.

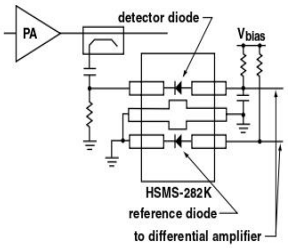


Figure 15. High Power Differential Detector.

The concept of the voltage doubler can be applied to the differential detector, permitting twice the output voltage for a given input power (as well as improving input impedance and suppressing second harmonics).

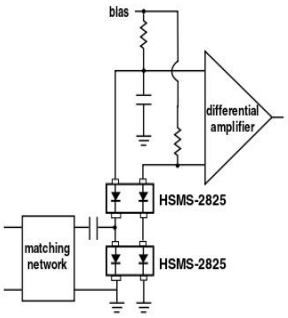


Figure 16. Voltage Doubler Differential Detector.

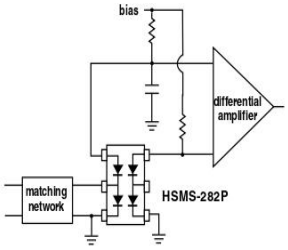


Figure 17. Voltage Doubler Differential Detector.

However, care must be taken to assure that the two reference diodes closely match the two detector diodes. One possible configuration is given in Figure 16, using two HSMS-2825. Board space can be saved through the use of the HSMS-282P open bridge quad, as shown in Figure 17.

While the differential detector works well over temperature, another design approach[3] works well for large signal detectors. See Figure 18 for the schematic and a physical layout of the circuit. In this design, the two 4.7 KΩ resistors and diode D2 act as a variable power divider, assuring constant output voltage over temperature and improving output linearity.

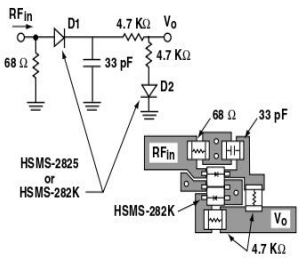


Figure 18. Temperature Compensated Detector.

In certain applications, such as a dual-band cellphone handset operating at both 900 and 1800 MHz, the second harmonics generated in the power control output detector when the handset is working at 900 MHz can cause problems. A filter at the output can reduce unwanted emissions at 1800 MHz in this case, but a lower cost solution is available[4]. Illustrated schematically in Figure 19, this circuit uses diode D2 and its associated passive components to cancel all even order harmonics at the detector's RF input. Diodes D3 and D4 provide temperature compensation as described above. All four diodes are contained in a single HSMS- 282R package, as illustrated in the layout shown in Figure 20.

[3] Hans Eriksson and Raymond W. Waugh, "A Temperature Compensated Linear Diode Detector," to be published.

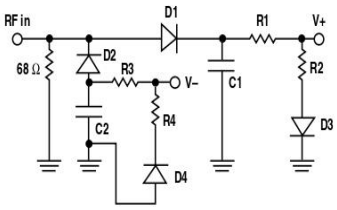


Figure 19. Schematic of Suppressed Harmonic Detector.

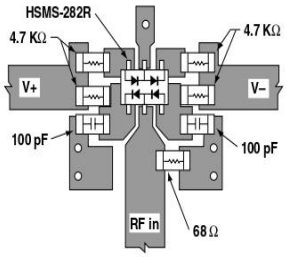


Figure 20. Layout of Suppressed Harmonic Detector.

Note that the forgoing discussion refers to the output voltage being extracted at point V+ with respect to ground. If a differential output is taken at V+ with respect to V-, the circuit acts as a voltage doubler.

Mixer applications

The HSMS-282x family, with its wide variety of packaging, can be used to make excellent mixers at frequencies up to 6 GHz.

The HSMS-2827 ring quad of matched diodes (in the SOT-143 package) has been designed for double balanced mixers. The smaller (SOT-363) HSMS-282R ring quad can similarly be used, if the quad is closed with external connections as shown in Figure 21.

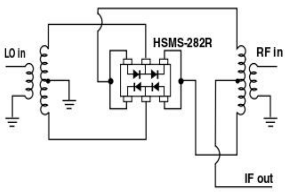


Figure 21. Double Balanced Mixer.

Both of these networks require a crossover or a three dimensional circuit. A planar mixer can be made using the SOT-143 crossover quad, HSMS-2829, as shown in Figure 22. In this product, a special lead frame permits the crossover to be placed inside the plastic package itself, eliminating the need for via holes (or other measures) in the RF portion of the circuit itself.

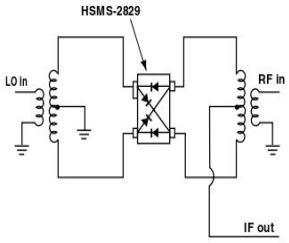


Figure 22. Planar Double Balanced Mixer.

A review of Figure 21 may lead to the question as to why the HSMS-282R ring quad is open on the ends. Distortion in double balanced mixers can be reduced if LO drive is increased, up to the point where the Schottky diodes are driven into saturation. Above this point, increased LO drive will not result in improvements in distortion. The use of expensive high barrier diodes (such as those fabricated on GaAs) can take advantage of higher LO drive power, but a lower cost solution is to use a eight (or twelve) diode ring quad. The open design of the HSMS-282R permits this to easily be done, as shown in Figure 23.

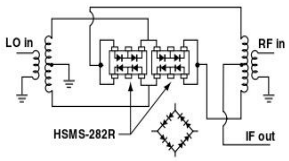


Figure 23. Low Distortion Double Balanced Mixer.

This same technique can be used in the single-balanced mixer. Figure 24 shows such a mixer, with two diodes in each spot normally occupied by one. This mixer, with a sufficiently high LO drive level, will display low distortion.

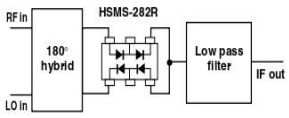


Figure 24. Low Distortion Balanced Mixer.

[4] Alan Rixon and Raymond W. Waugh, "A Suppressed Harmonic Power Detector for Dual Band 'Phones," to be published.

Sampling Applications

The six lead HSMS-282P can be used in a sampling circuit, as shown in Figure 25. As was the case with the six lead HSMS-282R in the mixer, the open bridge quad is closed with traces on the circuit board. The quad was not closed internally so that it could be used in other applications, such as illustrated in Figure 17.

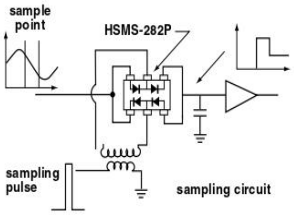


Figure 25. Sampling Circuit.

Thermal Considerations

The obvious advantage of the SOT-323 and SOT-363 over the SOT-23 and SOT-142 is combination of smaller size and extra leads. However, the copper leadframe in the SOT-3x3 has a thermal conductivity four times higher than the Alloy 42 leadframe of the SOT-23 and SOT-143, which enables the smaller packages to dissipate more power.

The maximum junction temperature for these three families of Schottky diodes is 150°C under all operating conditions. The following equation applies to the thermal analysis of diodes:

$$T_J = (V_f I_f + P_{RF})\,\theta_{jc} + T_a \qquad (1)$$

where

T_j = junction temperature

T_a = diode case temperature

θ_{jc} = thermal resistance

$V_f I_f$ = DC power dissipated

P_{RF} = RF power dissipated

Note that θ_{jc}, the thermal resistance from diode junction to the foot of the leads, is the sum of two component resistances,

$$\theta_{jc} = \theta_{pkg} + \theta_{chip} \qquad (2)$$

Package thermal resistance for the SOT-3x3 package is approximately 100°C/W, and the chip thermal resistance for the HSMS-282x family of diodes is approximately 40°C/W. The designer will have to add in the thermal resistance from diode case to ambient—a poor choice of circuit board material or heat sink design can make this number very high.

Equation (1) would be straightforward to solve but for the fact that diode forward voltage is a function of temperature as well as forward current. The equation for V_f is:

$$I_f = I_S \left[e^{\frac{11600\,(V_f - I_f R_s)}{nT}} - 1 \right] \qquad (3)$$

where

n = ideality factor

T = temperature in °K

R_s = diode series resistance

and I_S (diode saturation current) is given by

$$I_s = I_0 \left(\frac{T}{298}\right)^{\frac{2}{n}} e^{-4060\left(\frac{1}{T} - \frac{1}{298}\right)} \qquad (4)$$

Equation (4) is substituted into equation (3), and equations (1) and (3) are solved simultaneously to obtain the value of junction temperature for given values of diode case temperature, DC power dissipation and RF power dissipation.

Diode Burnout

Any Schottky junction, be it an RF diode or the gate of a MESFET, is relatively delicate and can be burned out with excessive RF power. Many crystal video receivers used in RFID (tag) applications find themselves in poorly controlled environments where high power sources may be present. Examples are the areas around airport and FAA radars, nearby ham radio operators, the vicinity of a broadcast band transmitter, etc. In such environments, the Schottky diodes of the receiver can be protected by a device known as a limiter diode.[5] Formerly available only in radar warning receivers and other high cost electronic warfare applications, these diodes have been adapted to commercial and consumer circuits.

Avago offers a complete line of surface mountable PIN limiter diodes. Most notably, our HSMP-4820 (SOT-23) can act as a very fast (nanosecond) power-sensitive switch when placed between the antenna and the Schottky diode, shorting out the RF circuit temporarily and reflecting the excessive RF energy back out the antenna.

[5] Avago Application Note 1050, "Low Cost, Surface Mount Power Limiters."

Assembly Instructions

SOT-3x3 PCB Footprint

Recommended PCB pad layouts for the miniature SOT-3x3 (SC-70) packages are shown in Figures 26 and 27 (dimensions are in inches). These layouts provide ample allowance for package placement by automated assembly equipment without adding parasitics that could impair the performance.

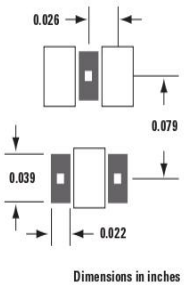


Figure 26. Recommended PCB Pad Layout for Avago's SC70 3L/SOT-323 Products.

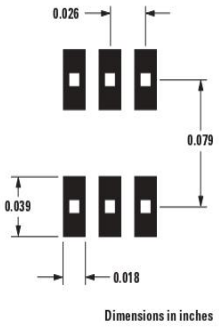


Figure 27. Recommended PCB Pad Layout for Avago's SC70 6L/SOT-363 Products.

SMT Assembly

Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g., IR or vapor phase reflow, wave soldering, etc.) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the SOT packages, will reach solder reflow temperatures faster than those with a greater mass.

Avago's diodes have been qualified to the time-temperature profile shown in Figure 28. This profile is representative of an IR reflow type of surface mount assembly process.

After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat zones. The preheat zones increase the temperature of the board and components to prevent thermal shock and begin evaporating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

The rates of change of temperature for the ramp-up and cool-down zones are chosen to be low enough to not cause deformation of the board or damage to components due to thermal shock. The maximum temperature in the reflow zone (T_{MAX}) should not exceed 260°C.

These parameters are typical for a surface mount assembly process for Avago diodes. As a general guideline, the circuit board and components should be exposed only to the minimum temperatures and times necessary to achieve a uniform reflow of solder.

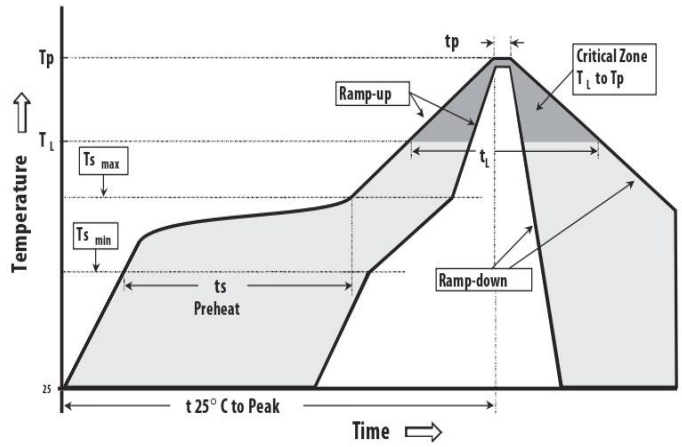


Figure 28. Surface Mount Assembly Profile.

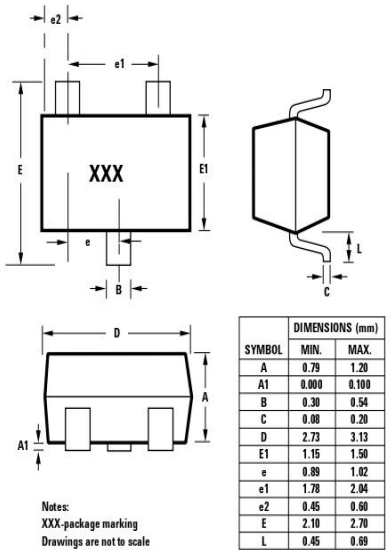
Lead-Free Reflow Profile Recommendation (IPC/JEDEC J-STD-020C)

Reflow Parameter		Lead-Free Assembly
Average ramp-up rate (Liquidus Temperature ($T_{S(max)}$ to Peak)		3°C/ second max
Preheat	Temperature Min ($T_{S(min)}$)	150°C
	Temperature Max ($T_{S(max)}$)	200°C
	Time (min to max) (t_S)	60-180 seconds
Ts(max) to TL Ramp-up Rate		3°C/second max
Time maintained above:	Temperature (T_L)	217°C
	Time (t_L)	60-150 seconds
Peak Temperature (T_p)		260 +0/-5°C
Time within 5 °C of actual Peak temperature (t_p)		20-40 seconds
Ramp-down Rate		6°C/second max
Time 25 °C to Peak Temperature		8 minutes max

Note 1: All temperatures refer to topside of the package, measured on the package body surface

Package Dimensions

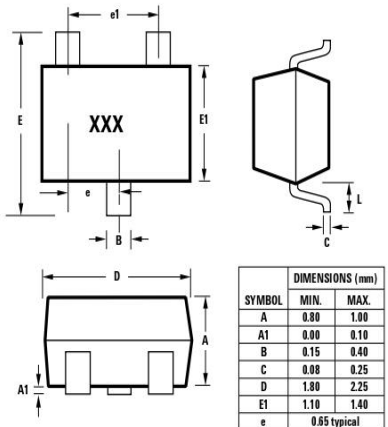
Outline 23 (SOT-23)



SYMBOL	DIMENSIONS (mm) MIN.	MAX.
A	0.79	1.20
A1	0.000	0.100
B	0.30	0.54
C	0.08	0.20
D	2.73	3.13
E1	1.15	1.50
e	0.89	1.02
e1	1.78	2.04
e2	0.45	0.60
E	2.10	2.70
L	0.45	0.69

Notes:
XXX-package marking
Drawings are not to scale

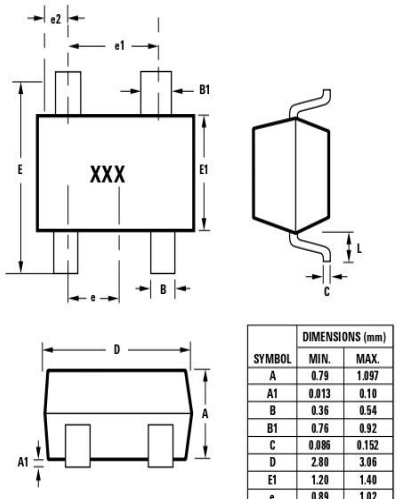
Outline SOT-323 (SC-70 3 Lead)



SYMBOL	DIMENSIONS (mm) MIN.	MAX.
A	0.80	1.00
A1	0.00	0.10
B	0.15	0.40
C	0.08	0.25
D	1.80	2.25
E1	1.10	1.40
e	0.65 typical	
e1	1.30 typical	
E	1.80	2.40
L	0.26	0.46

Notes:
XXX-package marking
Drawings are not to scale

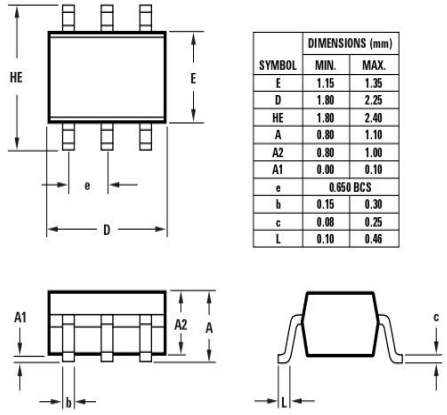
Outline 143 (SOT-143)



SYMBOL	DIMENSIONS (mm) MIN.	MAX.
A	0.79	1.097
A1	0.013	0.10
B	0.36	0.54
B1	0.76	0.92
C	0.086	0.152
D	2.80	3.06
E1	1.20	1.40
e	0.89	1.02
e1	1.78	2.04
e2	0.45	0.60
E	2.10	2.65
L	0.45	0.69

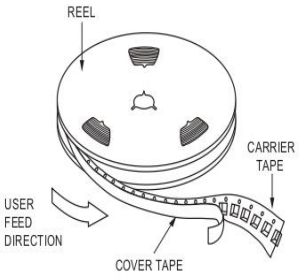
Notes:
XXX-package marking
Drawings are not to scale

Outline SOT-363 (SC-70 6 Lead)

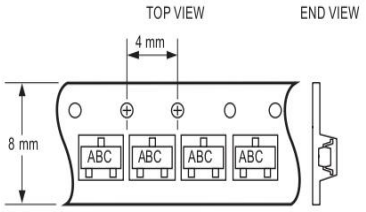


SYMBOL	DIMENSIONS (mm) MIN.	MAX.
E	1.15	1.35
D	1.80	2.25
HE	1.80	2.40
A	0.80	1.10
A2	0.80	1.00
A1	0.00	0.10
e	0.650 BCS	
b	0.15	0.30
c	0.08	0.25
L	0.10	0.46

Device Orientation

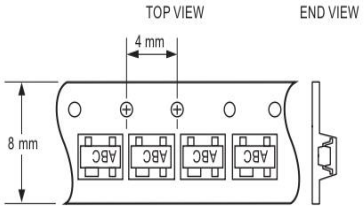


For Outlines SOT-23, -323



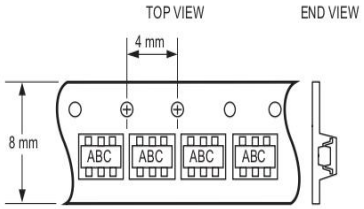
Note: "AB" represents package marking code.
"C" represents date code.

For Outline SOT-143



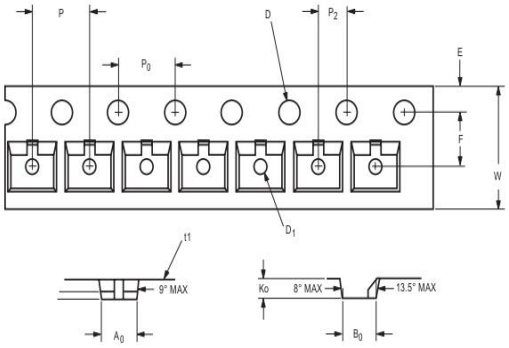
Note: "AB" represents package marking code.
"C" re presents date code.

For Outline SOT-363



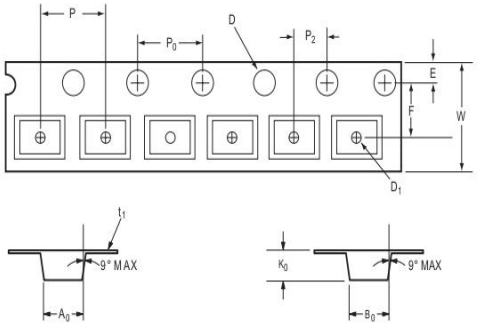
Note: "AB" represents package marking code.
"C" represents date code.

Tape Dimensions and Product Orientation For Outline SOT-23



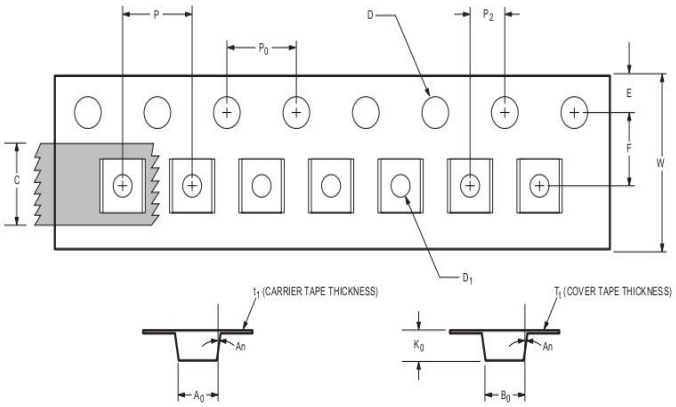
DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	3.15 ± 0.10	0.124 ± 0.004
	WIDTH	B_0	2.77 ± 0.10	0.109 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.05	0.039 ± 0.002
PERFORATION	DIAMETER	D	1.50 + 0.10	0.059 + 0.004
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 +0.30 −0.10	0.315+0.012 −0.004
	THICKNESS	t1	0.229 ± 0.013	0.009 ± 0.0005
DISTANCE BETWEEN CENTERLINE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

For Outline SOT-143



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	3.19 ± 0.10	0.126 ± 0.004
	WIDTH	B_0	2.80 ± 0.10	0.110 ± 0.004
	DEPTH	K_0	1.31 ± 0.10	0.052 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.50 + 0.10	0.059 + 0.004
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 +0.30 −0.10	0.315+0.012 −0.004
	THICKNESS	t1	0.254 ± 0.013	0.0100 ± 0.0005
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

Tape Dimensions and Product Orientation For Outlines SOT-323, -363



	DESCRIPTION	SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.40 ± 0.10	0.094 ± 0.004
	WIDTH	B_0	2.40 ± 0.10	0.094 ± 0.004
	DEPTH	K_0	1.20 ± 0.10	0.047 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.254 ± 0.02	0.0100 ± 0.0008
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002
ANGLE	FOR SOT-323 (SC70-3 LEAD)	An	8 °C MAX	
	FOR SOT-363 (SC70-6 LEAD)		10 °C MAX	

Part Number Ordering Information

Part Number	No. of Devices	Container
HSMS-282x-TR2G	10000	13" Reel
HSMS-282x-TR1G	3000	7" Reel
HSMS-282x-BLKG	100	antistatic bag

x = 0, 2, 3, 4, 5, 7, 8, 9, B, C, E, F, K, L, M, N, P or R

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

APPENDEIX B

HSMS-285x Series
Surface Mount Zero Bias Schottky Detector Diodes

AVAGO TECHNOLOGIES

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

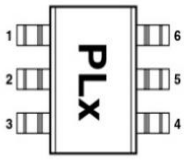
Description

Avago's HSMS-285x family of zero bias Schottky detector diodes has been designed and optimized for use in small signal (Pin <-20 dBm) applications at frequencies below 1.5 GHz. They are ideal for RF/ID and RF Tag applications where primary (DC bias) power is not available.

Important Note: For detector applications with input power levels greater than –20 dBm, use the HSMS-282x series at frequencies below 4.0 GHz, and the HSMS-286x series at frequencies above 4.0 GHz. The HSMS-285x series IS NOT RECOMMENDED for these higher power level applications.

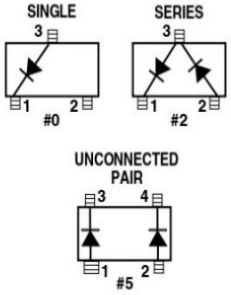
Available in various package configurations, these detector diodes provide low cost solutions to a wide variety of design problems. Avago's manufacturing techniques assure that when two diodes are mounted into a single package, they are taken from adjacent sites on the wafer, assuring the highest possible degree of match.

Pin Connections and Package Marking



Notes:
1. Package marking provides orientation and identification.
2. See "Electrical Specifications" for appropriate package marking.

SOT-23/SOT-143 Package Lead Code Identification (top view)



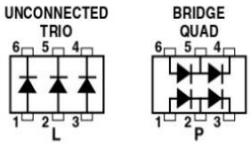
Features

- Surface Mount SOT-23/SOT-143 Packages
- Miniature SOT-323 and SOT-363 Packages
- High Detection Sensitivity:
  up to 50 mV/µW at 915 MHz
- Low Flicker Noise:
  -162 dBV/Hz at 100 Hz
- Low FIT (Failure in Time) Rate*
- Tape and Reel Options Available
- Matched Diodes for Consistent Performance
- Better Thermal Conductivity for Higher Power Dissipation
- Lead-free

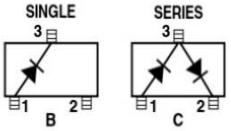
* For more information see the Surface Mount Schottky Reliability Data Sheet.

Attention: Observe precautions for handling electrostatic sensitive devices.
ESD Machine Model (Class A)
ESD Human Body Model (Class 0)
Refer to Avago Application Note A004R: Electrostatic Discharge Damage and Control.

SOT-363 Package Lead Code Identification (top view)



SOT-323 Package Lead Code Identification (top view)



SOT-23/SOT-143 DC Electrical Specifications, T_C = +25°C, Single Diode

Part Number HSMS-	Package Marking Code	Lead Code	Configuration	Maximum Forward Voltage V_F (mV)		Maximum Reverse Leakage, I_R (µA)	Typical Capacitance C_T (pF)
2850	P0	0	Single	150	250	175	0.30
2852	P2	2	Series Pair [1,2]				
2855	P5	5	Unconnected Pair[1,2]				
Test Conditions				I_F = 0.1 mA	I_F = 1.0 mA	V_R=2V	V_R = –0.5 V to –1.0V f = 1 MHz

Notes:
1. ΔVF for diodes in pairs is 15.0 mV maximum at 1.0 mA.
2. ΔCT for diodes in pairs is 0.05 pF maximum at –0.5V.

SOT-323/SOT-363 DC Electrical Specifications, T_C = +25°C, Single Diode

Part Number HSMS-	Package Marking Code	Lead Code	Configuration	Maximum Forward Voltage V_F (mV)		Maximum Reverse Leakage, I_R (µA)	Typical Capacitance C_T (pF)
285B	P0	B	Single	150	250	175.	0.30
285C	P2	C	Series Pair				
285L	PL	L	Unconnected Trio				
285P	PP	P	Bridge Quad				
Test Conditions				I_F = 0.1 mA	I_F = 1.0 mA	VR=2V	V_R = 0.5 V to –1.0V f = 1 MHz

Notes:
1. ΔVF for diodes in pairs is 15.0 mV maximum at 1.0 mA.
2. ΔCT for diodes in pairs is 0.05 pF maximum at –0.5V.

RF Electrical Specifications, T_C = +25°C, Single Diode

Part Number HSMS-	Typical Tangential Sensitivity TSS (dBm) @ f = 915 MHz	Typical Voltage Sensitivity g (mV/µW) @ f = 915 MHz	Typical Video Resistance RV (KΩ)
2850	–57	40	8.0
2852			
2855			
285B			
285C			
285L			
285P			
Test Conditions	Video Bandwidth = 2 MHz Zero Bias	Power in = –40 dBm R_L = 100 KΩ, Zero Bias	Zero Bias

Absolute Maximum Ratings, T_C = +25°C, Single Diode

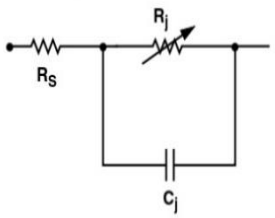
Symbol	Parameter	Unit	Absolute Maximum[1]	
			SOT-23/143	SOT-323/363
P_{IV}	Peak Inverse Voltage	V	2.0	2.0
T_J	Junction Temperature	°C	150	150
T_{STG}	Storage Temperature	°C	-65 to 150	-65 to 150
T_{OP}	Operating Temperature	°C	-65 to 150	-65 to 150
θ_{JC}	Thermal Resistance[2]	°C/W	500	150

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to the device.
2. T_C = +25°C, where T_C is defined to be the temperature at the package pins where contact is made to the circuit board.

ESD WARNING:
Handling Precautions Should Be Taken To Avoid Static Discharge.

Equivalent Linear Circuit Model

HSMS-285x chip



R_S = series resistance (see Table of SPICE parameters)

C_j = junction capacitance (see Table of SPICE parameters)

$$R_j = \frac{8.33 \times 10^{-5}\, nT}{I_b + I_s}$$

where

I_b = externally applied bias current in amps

I_s = saturation current (see table of SPICE parameters)

T = temperature, °K

n = ideality factor (see table of SPICE parameters)

Note:
To effectively model the packaged HSMS-285x product, please refer to Application Note AN1124.

SPICE Parameters

Parameter	Units	HSMS-285x
B_V	V	3.8
C_{J0}	pF	0.18
E_G	eV	0.69
I_{BV}	A	3 E-4
I_S	A	3 E-6
N		1.06
R_S	Ω	25
P_B (V_J)	V	0.35
P_T (XTI)		2
M		0.5

Typical Parameters, Single Diode

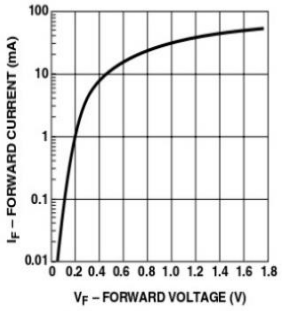


Figure 1. Typical Forward Current vs. Forward Voltage.

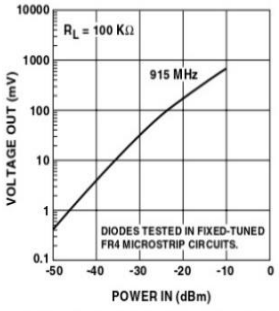


Figure 2. +25°C Output Voltage vs. Input Power at Zero Bias.

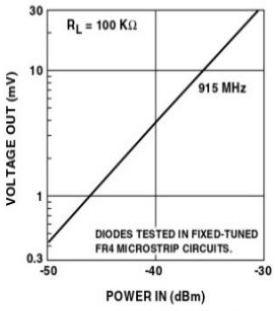


Figure 3. +25°C Expanded Output Voltage vs. Input Power. See Figure 2.

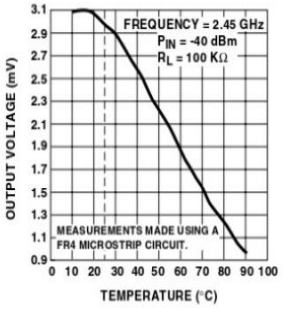


Figure 4. Output Voltage vs. Temperature.

Applications Information

Introduction

Avago's HSMS-285x family of Schottky detector diodes has been developed specifically for low cost, high volume designs in small signal (P_{in} < -20 dBm) applications at frequencies below 1.5 GHz. At higher frequencies, the DC biased HSMS-286x family should be considered.

In large signal power or gain control applications (P_{in} > -20 dBm), the HSMS-282x and HSMS-286x products should be used. The HSMS-285x zero bias diode is not designed for large signal designs.

Schottky Barrier Diode Characteristics

Stripped of its package, a Schottky barrier diode chip consists of a metal-semiconductor barrier formed by deposition of a metal layer on a semiconductor. The most common of several different types, the passivated diode, is shown in Figure 5, along with its equivalent circuit.

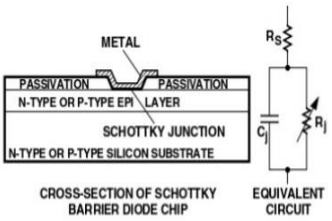


Figure 5. Schottky Diode Chip.

R_S is the parasitic series resistance of the diode, the sum of the bondwire and leadframe resistance, the resistance of the bulk layer of silicon, etc. RF energy coupled into R_S is lost as heat—it does not contribute to the rectified output of the diode. C_J is parasitic junction capacitance of the diode, controlled by the thickness of the epitaxial layer and the diameter of the Schottky contact. R_j is the junction resistance of the diode, a function of the total current flowing through it.

$$R_j = \frac{8.33 \times 10^{-5} n T}{I_s + I_b} = R_V - R_s$$

$$= \frac{0.026}{I_s + I_b} \text{ at } 25°C$$

where

n = ideality factor (see table of SPICE parameters)
T = temperature in °K
I_S = saturation current (see table of SPICE parameters)
I_b = externally applied bias current in amps

I_S is a function of diode barrier height, and can range from picoamps for high barrier diodes to as much as 5 µA for very low barrier diodes.

The Height of the Schottky Barrier

The current-voltage characteristic of a Schottky barrier diode at room temperature is described by the following equation:

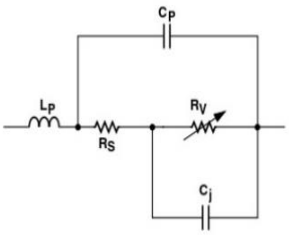
$$I = I_s \left(\exp\left(\frac{V - IR_s}{0.026}\right) - 1\right)$$

On a semi-log plot (as shown in the Avago catalog) the current graph will be a straight line with inverse slope 2.3 X 0.026 = 0.060 volts per cycle (until the effect of R_S is seen in a curve that droops at high current). All Schottky diode curves have the same slope, but not necessarily the same value of current for a given voltage. This is determined by the saturation current, I_S, and is related to the barrier height of the diode.

Through the choice of p-type or n-type silicon, and the selection of metal, one can tailor the characteristics of a Schottky diode. Barrier height will be altered, and at the same time C_J and R_S will be changed. In general, very low barrier height diodes (with high values of I_S, suitable for zero bias applications) are realized on p-type silicon. Such diodes suffer from higher values of R_S than do the n-type. Thus, p-type diodes are generally reserved for small signal detector applications (where very high values of R_V swamp out high R_S) and n-type diodes are used for mixer applications (where high L.O. drive levels keep R_V low).

Measuring Diode Parameters

The measurement of the five elements which make up the low frequency equivalent circuit for a packaged Schottky diode (see Figure 6) is a complex task. Various techniques are used for each element. The task begins with the elements of the diode chip itself.



FOR THE HSMS-285x SERIES
C_P = 0.08 pF
L_P = 2 nH
C_j = 0.18 pF
R_S = 25 Ω
R_V = 9 KΩ

Figure 6. Equivalent Circuit of a Schottky Diode.

R_S is perhaps the easiest to measure accurately. The V-I curve is measured for the diode under forward bias, and the slope of the curve is taken at some relatively high value of current (such as 5 mA). This slope is converted into a resistance R_d.

$$R_s = R_d - \frac{0.026}{I_f}$$

R_V and C_J are very difficult to measure. Consider the impedance of $C_J = 0.16$ pF when measured at 1 MHz — it is approximately 1 MΩ. For a well designed zero bias Schottky, R_V is in the range of 5 to 25 KΩ, and it shorts out the junction capacitance. Moving up to a higher frequency enables the measurement of the capacitance, but it then shorts out the video resistance. The best measurement technique is to mount the diode in series in a 50 Ω microstrip test circuit and measure its insertion loss at low power levels (around -20 dBm) using an HP8753C network analyzer. The resulting display will appear as shown in Figure 7.

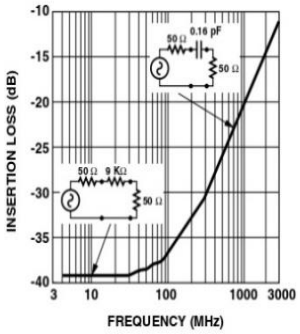


Figure 7. Measuring C_J and R_V.

At frequencies below 10 MHz, the video resistance dominates the loss and can easily be calculated from it. At frequencies above 300 MHz, the junction capacitance sets the loss, which plots out as a straight line when frequency is plotted on a log scale. Again, calculation is straightforward.

L_P and C_P are best measured on the HP8753C, with the diode terminating a 50 Ω line on the input port. The resulting tabulation of S_{11} can be put into a microwave linear analysis program having the five element equivalent circuit with R_V, C_J and R_S fixed. The optimizer can then adjust the values of L_P and C_P until the calculated S_{11} matches the measured values. Note that extreme care must be taken to de-embed the parasitics of the 50 Ω test fixture.

Detector Circuits

When DC bias is available, Schottky diode detector circuits can be used to create low cost RF and microwave receivers with a sensitivity of -55 dBm to -57 dBm.[1] These circuits can take a variety of forms, but in the most simple case they appear as shown in Figure 8. This is the basic detector circuit used with the HSMS-285x family of diodes.

In the design of such detector circuits, the starting point is the equivalent circuit of the diode, as shown in Figure 6.

Of interest in the design of the video portion of the circuit is the diode's video impedance—the other four elements of the equivalent circuit disappear at all reasonable video frequencies. In general, the lower the diode's video impedance, the better the design.

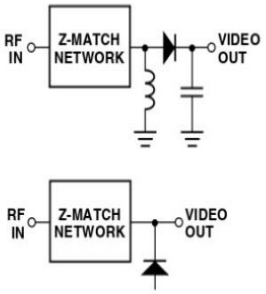


Figure 8. Basic Detector Circuits.

The situation is somewhat more complicated in the design of the RF impedance matching network, which includes the package inductance and capacitance (which can be tuned out), the series resistance, the junction capacitance and the video resistance. Of these five elements of the diode's equivalent circuit, the four parasitics are constants and the video resistance is a function of the current flowing through the diode.

$$R_V \approx \frac{26{,}000}{I_s + I_b}$$

where

I_S = diode saturation current in μA

I_b = bias current in μA

Saturation current is a function of the diode's design,[2] and it is a constant at a given temperature. For the HSMS-285x series, it is typically 3 to 5 μA at 25°C.

Saturation current sets the detection sensitivity, video resistance and input RF impedance of the zero bias Schottky detector diode. Since no external bias is used with the HSMS-285x series, a single transfer curve at any given frequency is obtained, as shown in Figure 2.

[1] Avago Application Note 923, Schottky Barrier Diode Video Detectors.

The most difficult part of the design of a detector circuit is the input impedance matching network. For very broadband detectors, a shunt 60 Ω resistor will give good input match, but at the expense of detection sensitivity.

When maximum sensitivity is required over a narrow band of frequencies, a reactive matching network is optimum. Such networks can be realized in either lumped or distributed elements, depending upon frequency, size constraints and cost limitations, but certain general design principals exist for all types.[3] Design work begins with the RF impedance of the HSMS-285x series, which is given in Figure 9.

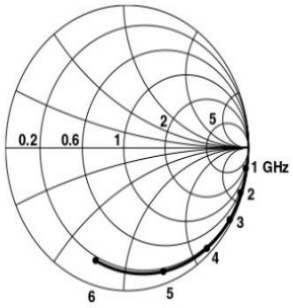


Figure 9. RF Impedance of the HSMS-285x Series at -40 dBm.

915 MHz Detector Circuit

Figure 10 illustrates a simple impedance matching network for a 915 MHz detector.

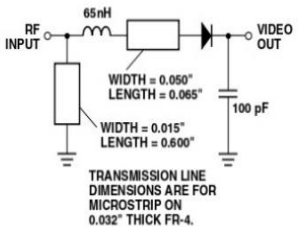


Figure 10. 915 MHz Matching Network for the HSMS-285x Series at Zero Bias.

A 65 nH inductor rotates the impedance of the diode to a point on the Smith Chart where a shunt inductor can pull it up to the center. The short length of 0.065" wide microstrip line is used to mount the lead of the diode's SOT-323 package. A shorted shunt stub of length <λ/4 provides the necessary shunt inductance and simultaneously provides the return circuit for the current generated in the diode. The impedance of this circuit is given in Figure 11.

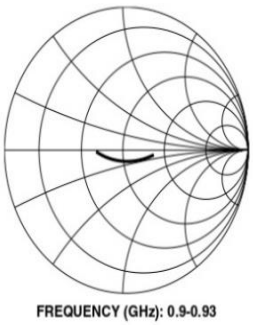


Figure 11. Input Impedance.

The input match, expressed in terms of return loss, is given in Figure 12.

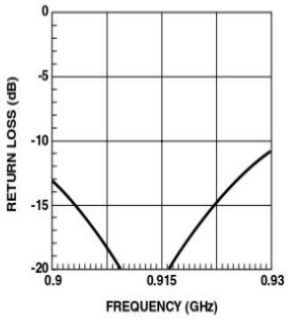


Figure 12. Input Return Loss.

As can be seen, the band over which a good match is achieved is more than adequate for 915 MHz RFID applications.

Voltage Doublers

To this point, we have restricted our discussion to single diode detectors. A glance at Figure 8, however, will lead to the suggestion that the two types of single diode detectors be combined into a two diode voltage doubler[4] (known also as a full wave rectifier). Such a detector is shown in Figure 13.

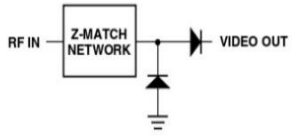


Figure 13. Voltage Doubler Circuit.

[2] Avago Application Note 969, An Optimum Zero Bias Schottky Detector Diode.
[3] Avago Application Note 963, Impedance Matching Techniques for Mixers and Detectors.

Such a circuit offers several advantages. First the voltage outputs of two diodes are added in series, increasing the overall value of voltage sensitivity for the network (compared to a single diode detector). Second, the RF impedances of the two diodes are added in parallel, making the job of reactive matching a bit easier. Such a circuit can easily be realized using the two series diodes in the HSMS-285C.

Flicker Noise

Reference to Figure 5 will show that there is a junction of metal, silicon, and passivation around the rim of the Schottky contact. It is in this three-way junction that flicker noise[5] is generated. This noise can severely reduce the sensitivity of a crystal video receiver utilizing a Schottky detector circuit if the video frequency is below the noise corner. Flicker noise can be substantially reduced by the elimination of passivation, but such diodes cannot be mounted in non-hermetic packages. p-type silicon Schottky diodes have the least flicker noise at a given value of external bias (compared to n-type silicon or GaAs). At zero bias, such diodes can have extremely low values of flicker noise. For the HSMS-285x series, the noise temperature ratio is given in Figure 14.

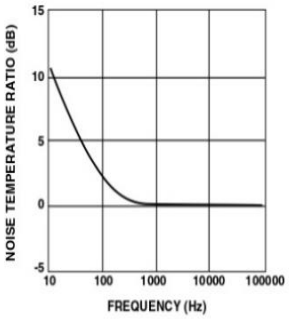


Figure 14. Typical Noise Temperature Ratio.

Diode Burnout

Noise temperature ratio is the quotient of the diode's noise power (expressed in dBV/Hz) divided by the noise power of an ideal resistor of resistance $R = R_V$.

For an ideal resistor R, at 300°K, the noise voltage can be computed from

$$v = 1.287 \times 10^{-10} \sqrt{R} \text{ volts/Hz}$$

which can be expressed as

$$20 \log_{10} v \quad \text{dBV/Hz}$$

Thus, for a diode with R_V = 9KΩ, the noise voltage is 12.2 nV/Hz or -158 dBV/Hz. On the graph of Figure 14, -158 dBV/Hz would replace the zero on the vertical scale to convert the chart to one of absolute noise voltage vs. frequency.

Any Schottky junction, be it an RF diode or the gate of a MESFET, is relatively delicate and can be burned out with excessive RF power. Many crystal video receivers used in RFID (tag) applications find themselves in poorly controlled environments where high power sources may be present. Examples are the areas around airport and FAA radars, nearby ham radio operators, the vicinity of a broadcast band transmitter, etc. In such environments, the Schottky diodes of the receiver can be protected by a device known as a limiter diode.[6] Formerly available only in radar warning receivers and other high cost electronic warfare applications, these diodes have been adapted to commercial and consumer circuits.

Avago offers a complete line of surface mountable PIN limiter diodes. Most notably, our HSMP-4820 (SOT-23) can act as a very fast (nanosecond) power-sensitive switch when placed between the antenna and the Schottky diode, shorting out the RF circuit temporarily and reflecting the excessive RF energy back out the antenna.

Assembly Instructions

SOT-323 PCB Footprint

A recommended PCB pad layout for the miniature SOT-323 (SC-70) package is shown in Figure 15 (dimensions are in inches). This layout provides ample allowance for package placement by automated assembly equipment without adding parasitics that could impair the performance. Figure 16 shows the pad layout for the six-lead SOT-363.

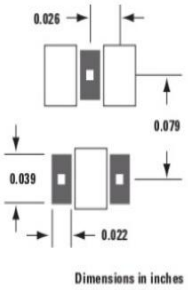


Figure 15. Recommended PCB Pad Layout for Avago's SC70 3L/SOT-323 Products.

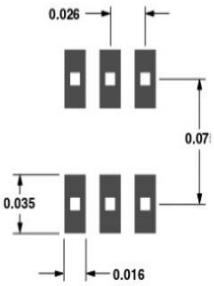


Figure 16. Recommended PCB Pad Layout for Avago's SC70 6L/SOT-363 Products.

[4] Avago Application Note 956-4, Schottky Diode Voltage Doubler.
[5] Avago Application Note 965-3, Flicker Noise in Schottky Diodes.
[6] Avago Application Note 1050, Low Cost, Surface Mount Power Limiters.

SMT Assembly

Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g., IR or vapor phase reflow, wave soldering, etc.) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the SOT packages, will reach solder reflow temperatures faster than those with a greater mass.

Avago's diodes have been qualified to the time-temperature profile shown in Figure 17. This profile is representative of an IR reflow type of surface mount assembly process.

After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat zones. The preheat zones increase the temperature of the board and components to prevent thermal shock and begin evaporating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

The rates of change of temperature for the ramp-up and cool-down zones are chosen to be low enough to not cause deformation of the board or damage to components due to thermal shock. The maximum temperature in the reflow zone (T_{MAX}) should not exceed 260°C.

These parameters are typical for a surface mount assembly process for Avago diodes. As a general guideline, the circuit board and components should be exposed only to the minimum temperatures and times necessary to achieve a uniform reflow of solder.

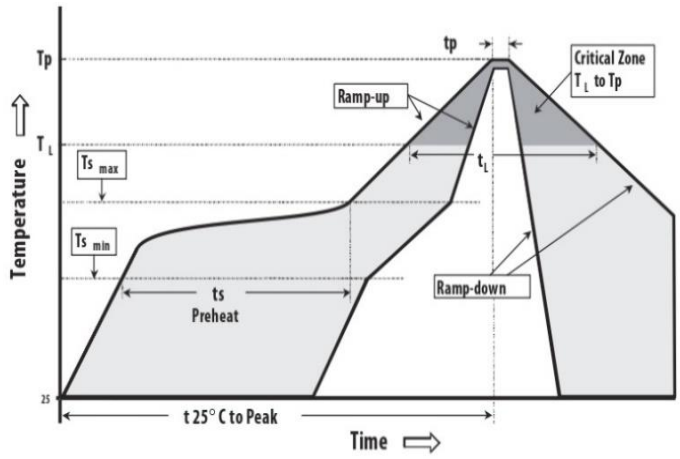


Figure 17. Surface Mount Assembly Profile.

Lead-Free Reflow Profile Recommendation (IPC/JEDEC J-STD-020C)

Reflow Parameter		Lead-Free Assembly
Average ramp-up rate (Liquidus Temperature ($T_{S(max)}$ to Peak)		3°C/ second max
Preheat	Temperature Min ($T_{S(min)}$)	150°C
	Temperature Max ($T_{S(max)}$)	200°C
	Time (min to max) (t_S)	60-180 seconds
Ts(max) to TL Ramp-up Rate		3°C/second max
Time maintained above:	Temperature (T_L)	217°C
	Time (t_L)	60-150 seconds
Peak Temperature (T_P)		260 +0/-5°C
Time within 5 °C of actual Peak temperature (t_P)		20-40 seconds
Ramp-down Rate		6°C/second max
Time 25 °C to Peak Temperature		8 minutes max

Note 1: All temperatures refer to topside of the package, measured on the package body surface

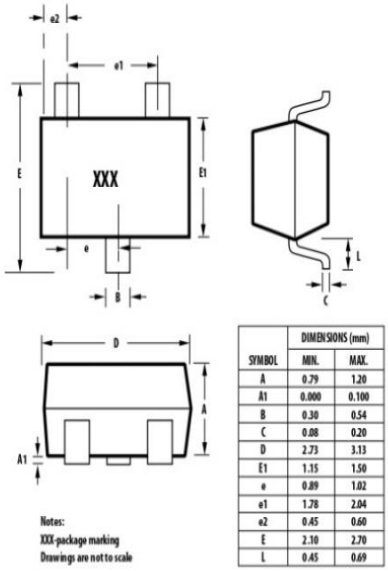
Part Number Ordering Information

Part Number	No. of Devices	Container
HSMS-285x-TR2G	10000	13" Reel
HSMS-285x-TR1G	3000	7" Reel
HSMS-285x-BLKG	100	antistatic bag

where x = 0, 2, 5, B, C, L and P for HSMS-285x.

Package Dimensions

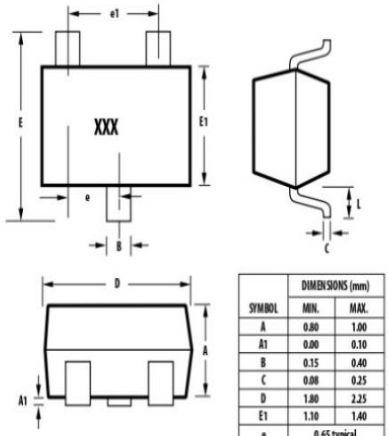
Outline 23 (SOT-23)



Notes:
XXX-package marking
Drawings are not to scale

SYMBOL	DIMENSIONS (mm) MIN.	MAX.
A	0.79	1.20
A1	0.000	0.100
B	0.30	0.54
C	0.08	0.20
D	2.73	3.13
E1	1.15	1.50
e	0.89	1.02
e1	1.78	2.04
e2	0.45	0.60
E	2.10	2.70
L	0.45	0.69

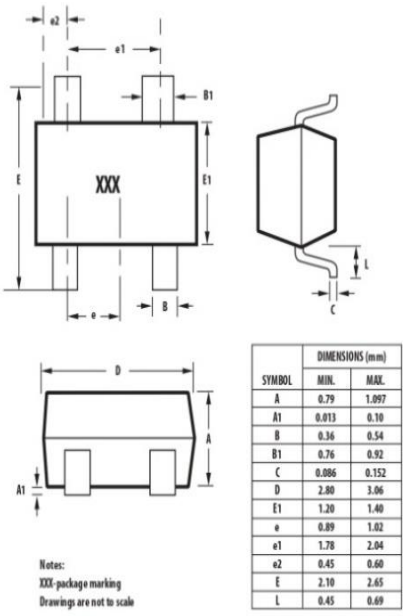
Outline SOT-323 (SC-70 3 Lead)



Notes:
XXX-package marking
Drawings are not to scale

SYMBOL	DIMENSIONS (mm) MIN.	MAX.
A	0.80	1.00
A1	0.00	0.10
B	0.15	0.40
C	0.08	0.25
D	1.80	2.25
E1	1.10	1.40
e	0.65 typical	
e1	1.30 typical	
E	1.80	2.40
L	0.26	0.46

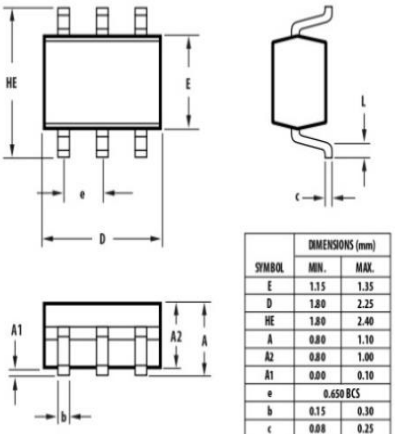
Outline 143 (SOT-143)



SYMBOL	DIMENSIONS (mm) MIN.	MAX.
A	0.79	1.097
A1	0.013	0.10
B	0.36	0.54
B1	0.76	0.92
C	0.086	0.152
D	2.80	3.06
E1	1.20	1.40
e	0.89	1.02
e1	1.78	2.04
e2	0.45	0.60
E	2.10	2.65
L	0.45	0.69

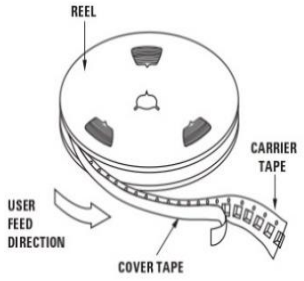
Notes:
XXX-package marking
Drawings are not to scale

Outline SOT-363 (SC-70 6 Lead)

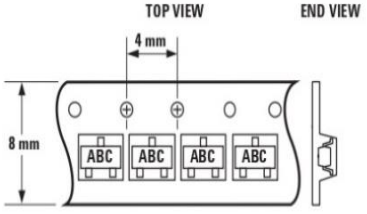


SYMBOL	DIMENSIONS (mm) MIN.	MAX.
E	1.15	1.35
D	1.80	2.25
HE	1.80	2.40
A	0.80	1.10
A2	0.80	1.00
A1	0.00	0.10
e	0.650 BCS	
b	0.15	0.30
c	0.08	0.25
L	0.10	0.46

Device Orientation

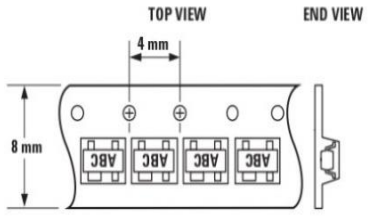


For Outlines SOT-23, -323



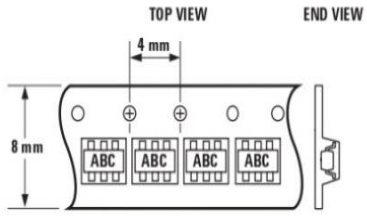
Note: "AB" represents package marking code.
"C" represents date code.

For Outline SOT-143



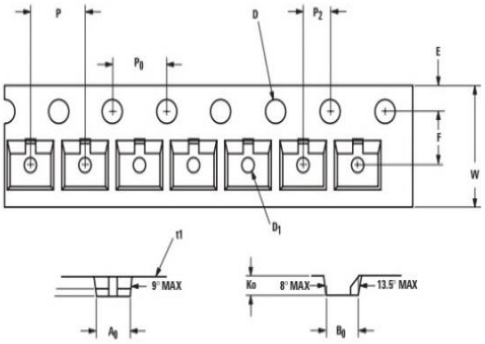
Note: "AB" represents package marking code.
"C" represents date code.

For Outline SOT-363



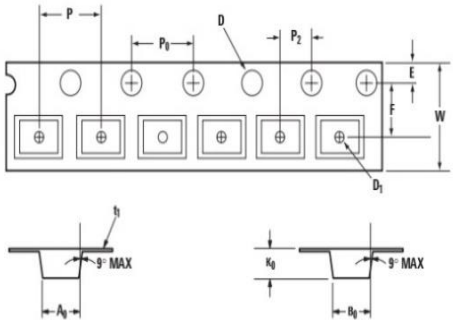
Note: "AB" represents package marking code.
"C" represents date code.

Tape Dimensions and Product Orientation
For Outline SOT-23



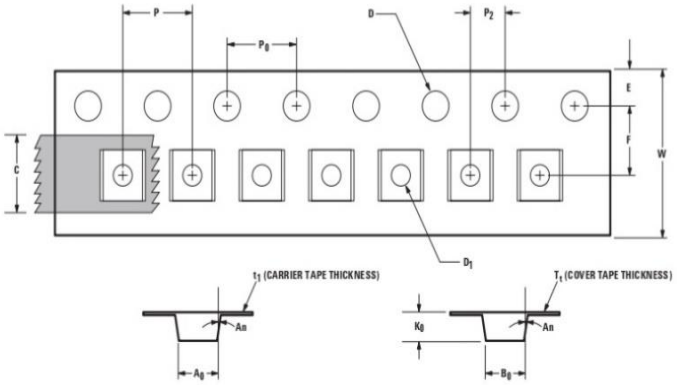
DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	3.15 ± 0.10	0.124 ± 0.004
	WIDTH	B_0	2.77 ± 0.10	0.109 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.05	0.039 ± 0.002
PERFORATION	DIAMETER	D	1.50 + 0.10	0.059 + 0.004
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 +0.30 –0.10	0.315 +0.012 –0.004
	THICKNESS	t1	0.229 ± 0.013	0.009 ± 0.0005
DISTANCE BETWEEN CENTERLINE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

For Outline SOT-143



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	3.19 ± 0.10	0.126 ± 0.004
	WIDTH	B_0	2.80 ± 0.10	0.110 ± 0.004
	DEPTH	K_0	1.31 ± 0.10	0.052 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.50 + 0.10	0.059 + 0.004
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 + 0.30 – 0.10	0.315 + 0.012 – 0.004
	THICKNESS	t1	0.254 ± 0.013	0.0100 ± 0.0005
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

Tape Dimensions and Product Orientation
For Outlines SOT-323, -363



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.40 ± 0.10	0.094 ± 0.004
	WIDTH	B_0	2.40 ± 0.10	0.094 ± 0.004
	DEPTH	K_0	1.20 ± 0.10	0.047 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.254 ± 0.02	0.0100 ± 0.0008
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_1	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002
ANGLE	FOR SOT-323 (SC70-3 LEAD)	An	8° C MAX	
	FOR SOT-363 (SC70-6 LEAD)		10° C MAX	

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

AV02-1377EN - May 29, 2009

AVAGO TECHNOLOGIES

APPENDEIX C

HSMS-286x Series
Surface Mount Microwave Schottky Detector Diodes

AVAGO TECHNOLOGIES

Data Sheet

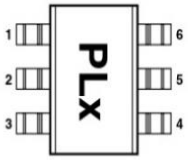
Lead (Pb) Free
RoHS 6 fully compliant

Description

Avago's HSMS-286x family of DC biased detector diodes have been designed and optimized for use from 915 MHz to 5.8 GHz. They are ideal for RF/ID and RF Tag applications as well as large signal detection, modulation, RF to DC conversion or voltage doubling.

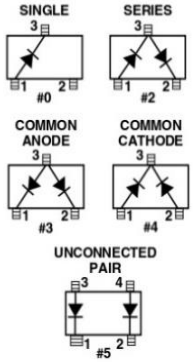
Available in various package configurations, this family of detector diodes provides low cost solutions to a wide variety of design problems. Avago's manufacturing techniques assure that when two or more diodes are mounted into a single surface mount package, they are taken from adjacent sites on the wafer, assuring the highest possible degree of match.

Pin Connections and Package Marking



Notes:
1. Package marking provides orientation and identification.
2. The first two characters are the package marking code. The third character is the date code.

SOT-23/SOT-143 Package Lead Code Identification (top view)

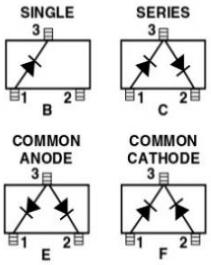


Features

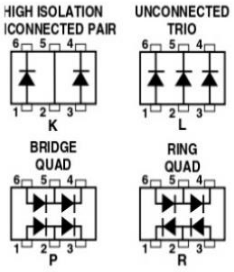
- Surface Mount SOT-23/SOT-143 Packages
- Miniature SOT-323 and SOT-363 Packages
- High Detection Sensitivity:
  up to 50 mV/µW at 915 MHz
  up to 35 mV/µW at 2.45 GHz
  up to 25 mV/µW at 5.80 GHz
- Low FIT (Failure in Time) Rate*
- Tape and Reel Options Available
- Unique Configurations in Surface Mount SOT-363 Package
  – increase flexibility
  – save board space
  – reduce cost
- HSMS-286K Grounded Center Leads Provide up to 10 dB Higher Isolation
- Matched Diodes for Consistent Performance
- Better Thermal Conductivity for Higher Power Dissipation
- Lead-free

* For more information see the Surface Mount Schottky Reliability Data Sheet.

SOT-323 Package Lead Code Identification (top view)



SOT-363 Package Lead Code Identification (top view)



SOT-23/SOT-143 DC Electrical Specifications, T_C = +25°C, Single Diode

Part Number HSMS-	Package Marking Code	Lead Code	Configuration	Forward Voltage V_F (mV)		Typical Capacitance C_T (pF)
2860	T0	0	Single	250 Min.	350 Max.	0.30
2862	T2	2	Series Pair[1,2]			
2863	T3	3	Common Anode[1,2]			
2864	T4	4	Common Cathode[1,2]			
2865	T5	5	Unconnected Pair[1,2]			
Test Conditions				I_F = 1.0 mA		V_R = 0 V, f = 1 MHz

Notes:
1. ΔVF for diodes in pairs is 15.0 mV maximum at 1.0 mA.
2. ΔCT for diodes in pairs is 0.05 pF maximum at –0.5V.

SOT-323/SOT-363 DC Electrical Specifications, T_C = +25°C, Single Diode

Part Number HSMS-	Package Marking Code	Lead Code	Configuration	Forward Voltage V_F (mV)		Typical Capacitance C_T (pF)
286B	T0	B	Single	250 Min.	350 Max.	0.25
286C	T2	C	Series Pair[1,2]			
286E	T3	E	Common Anode[1,2]			
286F	T4	F	Common Cathode[1,2]			
286K	TK	K	High Isolation Unconnected Pair			
286L	TL	L	Unconnected Trio			
286P	TP	P	Bridge Quad			
286R	ZZ	R	Ring Quad			
Test Conditions				I_F = 1.0 mA		V_R = 0 V, f = 1 MHz

Notes:
1. ΔVF for diodes in pairs is 15.0 mV maximum at 1.0 mA.
2. ΔCT for diodes in pairs is 0.05 pF maximum at –0.5V.

RF Electrical Specifications, T_C = +25°C, Single Diode

Part Number HSMS-	Typical Tangential Sensitivity TSS (dBm) @ f = 915 MHz	2.45 GHz	5.8 GHz	Typical Voltage Sensitivity g (mV/µW) @ f = 915 MHz	2.45 GHz	5.8 GHz	Typical Video Resistance RV (KΩ)
2860	–57	–56	–55	50	35	25	5.0
2862							
2863							
2864							
2865							
286B							
286C							
286E							
286F							
286K							
286L							
286P							
286R							
Test Conditions	Video Bandwidth = 2 MHz I_b = 5 µA			Power in = –40 dBm R_L = 100 KΩ, I_b = 5 µA			I_b = 5 µA

Absolute Maximum Ratings, T_C = +25°C, Single Diode

Symbol	Parameter	Unit	Absolute Maximum[1] SOT-23/143	SOT-323/363
P_{IV}	Peak Inverse Voltage	V	4.0	4.0
T_J	Junction Temperature	°C	150	150
T_{STG}	Storage Temperature	°C	-65 to 150	-65 to 150
T_{OP}	Operating Temperature	°C	-65 to 150	-65 to 150
θ_{JC}	Thermal Resistance[2]	°C/W	500	150

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to the device.
2. T_C = +25°C, where T_C is defined to be the temperature at the package pins where contact is made to the circuit board.

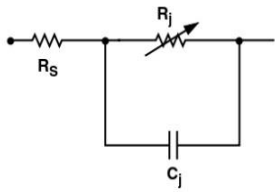
Attention:
Observe precautions for handling electrostatic sensitive devices.

ESD Machine Model (Class A)

ESD Human Body Model (Class 0)

Refer to Avago Application Note A004R: Electrostatic Discharge Damage and Control.

Equivalent Linear Circuit Model, Diode chip



R_S = series resistance (see Table of SPICE parameters)

C_j = junction capacitance (see Table of SPICE parameters)

$$R_j = \frac{8.33 \times 10^{-5}\, nT}{I_b + I_s}$$

where

I_b = externally applied bias current in amps

I_s = saturation current (see table of SPICE parameters)

T = temperature, °K

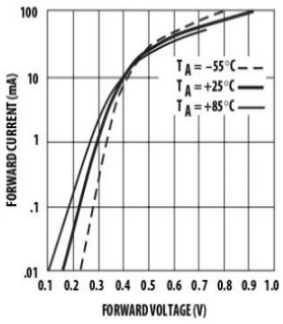
n = ideality factor (see table of SPICE parameters)

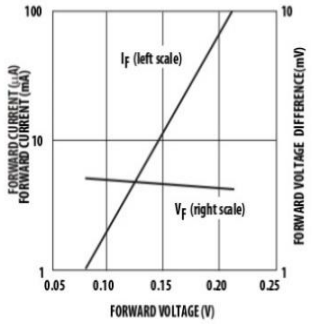
Note:
To effectively model the packaged HSMS-286x product, please refer to Application Note AN1124.

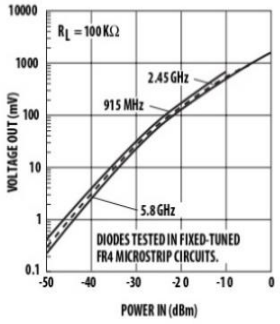
SPICE Parameters

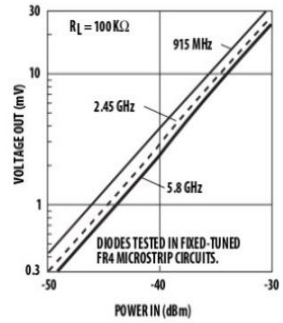
Parameter	Units	Value
B_V	V	7.0
C_{J0}	pF	0.18
E_G	eV	0.69
I_{BV}	A	1 E - 5
I_S	A	5 E - 8
N		1.08
R_S	Ω	6.0
P_B (VJ)	V	0.65
P_T (XTI)		2
M		0.5

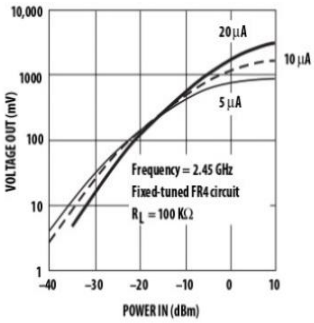
Typical Parameters, Single Diode

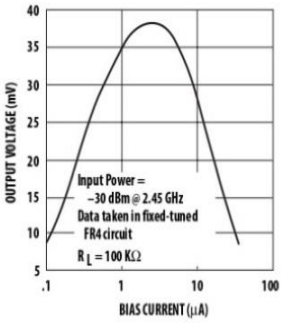












Applications Information

Introduction

Avago's HSMS-286x family of Schottky detector diodes has been developed specifically for low cost, high volume designs in two kinds of applications. In small signal detector applications (P_{in} < -20 dBm), this diode is used with DC bias at frequencies above 1.5 GHz. At lower frequencies, the zero bias HSMS-285x family should be considered.

In large signal power or gain control applications (P_{in} > -20 dBm), this family is used without bias at frequencies above 4 GHz. At lower frequencies, the HSMS-282x family is preferred.

Schottky Barrier Diode Characteristics

Stripped of its package, a Schottky barrier diode chip consists of a metal-semiconductor barrier formed by deposition of a metal layer on a semiconductor. The most common of several different types, the passivated diode, is shown in Figure 7, along with its equivalent circuit.

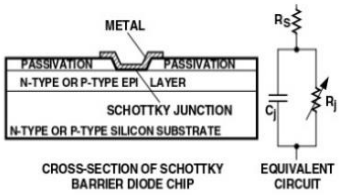


Figure 7. Schottky Diode Chip.

R_S is the parasitic series resistance of the diode, the sum of the bondwire and leadframe resistance, the resistance of the bulk layer of silicon, etc. RF energy coupled into R_S is lost as heat — it does not contribute to the rectified output of the diode. C_J is parasitic junction capacitance of the diode, controlled by the thickness of the epitaxial layer and the diameter of the Schottky contact. R_j is the junction resistance of the diode, a function of the total current flowing through it.

$$R_j = \frac{8.33 \times 10^{-5} n T}{I_S + I_b} = R_V - R_s$$

$$= \frac{0.026}{I_S + I_b} \text{ at } 25°C$$

where

n = ideality factor (see table of SPICE parameters)
T = temperature in °K
I_S = saturation current (see table of SPICE parameters)
I_b = externally applied bias current in amps

I_S is a function of diode barrier height, and can range from picoamps for high barrier diodes to as much as 5 µA for very low barrier diodes.

The Height of the Schottky Barrier

The current-voltage characteristic of a Schottky barrier diode at room temperature is described by the following equation:

$$I = I_S \left(\exp\left(\frac{V - IR_S}{0.026}\right) - 1\right)$$

On a semi-log plot (as shown in the Avago catalog) the current graph will be a straight line with inverse slope 2.3 X 0.026 = 0.060 volts per cycle (until the effect of R_S is seen in a curve that droops at high current). All Schottky diode curves have the same slope, but not necessarily the same value of current for a given voltage. This is determined by the saturation current, I_S, and is related to the barrier height of the diode.

Through the choice of p-type or n-type silicon, and the selection of metal, one can tailor the characteristics of a Schottky diode. Barrier height will be altered, and at the same time C_J and R_S will be changed. In general, very low barrier height diodes (with high values of I_S, suitable for zero bias applications) are realized on p-type silicon. Such diodes suffer from higher values of R_S than do the n-type. Thus, p-type diodes are generally reserved for small signal detector applications (where very high values of R_V swamp out high R_S) and n-type diodes are used for mixer applications (where high L.O. drive levels keep R_V low) and DC biased detectors.

Measuring Diode Linear Parameters

The measurement of the many elements which make up the equivalent circuit for a packaged Schottky diode is a complex task. Various techniques are used for each element. The task begins with the elements of the diode chip itself. (See Figure 8).

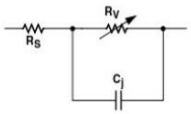


Figure 8. Equivalent Circuit of a Schottky Diode Chip.

R_S is perhaps the easiest to measure accurately. The V-I curve is measured for the diode under forward bias, and the slope of the curve is taken at some relatively high value of current (such as 5 mA). This slope is converted into a resistance R_d.

$$R_S = R_d - \frac{0.026}{I_f}$$

For n-type diodes with relatively low values of saturation current, C_j is obtained by measuring the total capacitance (see AN1124). R_j, the junction resistance, is calculated using the equation given above.

The characterization of the surface mount package is too complex to describe here—linear equivalent circuits can be found in AN1124.

Detector Circuits (small signal)

When DC bias is available, Schottky diode detector circuits can be used to create low cost RF and microwave receivers with a sensitivity of -55 dBm to -57 dBm.[1] Moreover, since external DC bias sets the video impedance of such circuits, they display classic square law response over a wide range of input power levels[2,3]. These circuits can take a variety of forms, but in the most simple case they appear as shown in Figure 9. This is the basic detector circuit used with the HSMS-286x family of diodes.

Output voltage can be virtually doubled and input impedance (normally very high) can be halved through the use of the voltage doubler circuit[4].

In the design of such detector circuits, the starting point is the equivalent circuit of the diode. Of interest in the design of the video portion of the circuit is the diode's video impedance—the other elements of the equivalent circuit disappear at all reasonable video frequencies. In general, the lower the diode's video impedance, the better the design.

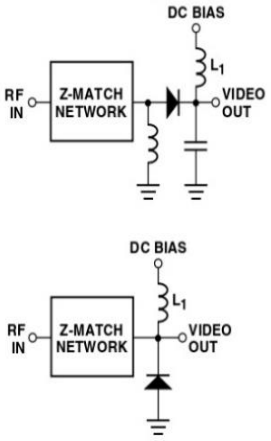


Figure 9. Basic Detector Circuits.

The situation is somewhat more complicated in the design of the RF impedance matching network, which includes the package inductance and capacitance (which can be tuned out), the series resistance, the junction capacitance and the video resistance. Of the elements of the diode's equivalent circuit, the parasitics are constants and the video resistance is a function of the current flowing through the diode.

$$R_V = R_j + R_S$$

The sum of saturation current and bias current sets the detection sensitivity, video resistance and input RF impedance of the Schottky detector diode. Where bias current is used, some tradeoff in sensitivity and square law dynamic range is seen, as shown in Figure 5 and described in reference [3].

The most difficult part of the design of a detector circuit is the input impedance matching network. For very broadband detectors, a shunt 60 Ω resistor will give good input match, but at the expense of detection sensitivity.

When maximum sensitivity is required over a narrow band of frequencies, a reactive matching network is optimum. Such networks can be realized in either lumped or distributed elements, depending upon frequency, size constraints and cost limitations, but certain general design principals exist for all types.[5] Design work begins with the RF impedance of the HSMS-286x series when bias current is set to 3 µA. See Figure 10.

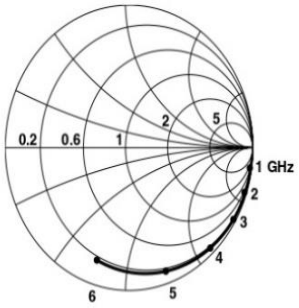


Figure 10. RF Impedance of the Diode.

[1] Avago Application Note 923, Schottky Barrier Diode Video Detectors.
[2] Avago Application Note 986, Square Law and Linear Detection.
[3] Avago Application Note 956-5, Dynamic Range Extension of Schottky Detectors.
[4] Avago Application Note 956-4, Schottky Diode Voltage Doubler.
[5] Avago Application Note 963, Impedance Matching Techniques for Mixers and Detectors.

915 MHz Detector Circuit

Figure 11 illustrates a simple impedance matching network for a 915 MHz detector.

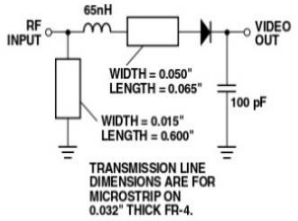


Figure 11. 915 MHz Matching Network for the HSMS-286x Series at 3 µA Bias.

A 65 nH inductor rotates the impedance of the diode to a point on the Smith Chart where a shunt inductor can pull it up to the center. The short length of 0.065" wide microstrip line is used to mount the lead of the diode's SOT-323 package. A shorted shunt stub of length <λ/4 provides the necessary shunt inductance and simultaneously provides the return circuit for the current generated in the diode. The impedance of this circuit is given in Figure 12.

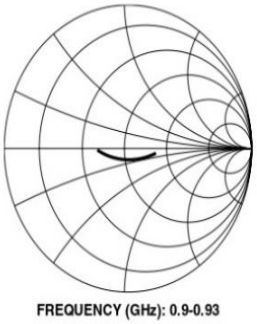


Figure 12. Input Impedance.

The input match, expressed in terms of return loss, is given in Figure 13.

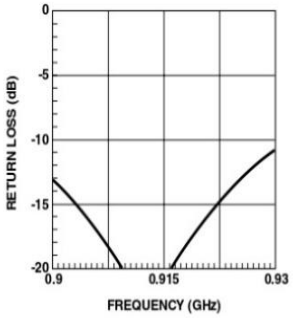


Figure 13. Input Return Loss.

As can be seen, the band over which a good match is achieved is more than adequate for 915 MHz RFID applications.

The HSMS-282x family is a better choice for 915 MHz applications—the foregoing discussion of a design using the HSMS-286B is offered only to illustrate a design approach for technique.

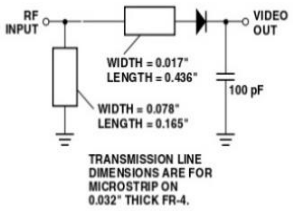


Figure 14. 2.45 GHz Matching Network.

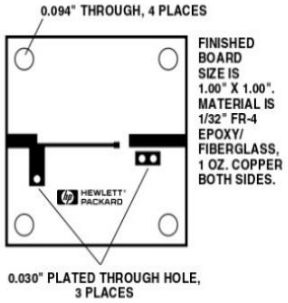


Figure 15. Physical Realization.

2.45 GHz Detector Circuit

At 2.45 GHz, the RF impedance is closer to the line of constant susceptance which passes through the center of the chart, resulting in a design which is realized entirely in distributed elements — see Figure 14.

In order to save cost (at the expense of having a larger circuit), an open circuit shunt stub could be substituted for the chip capacitor. On the other hand, if space is at a premium, the long series transmission line at the input to the diode can be replaced with a lumped inductor. A possible physical realization of such a network is shown in Figure 15, a demo board is available from Avago.

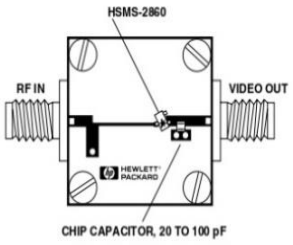


Figure 16. Test Detector.

Two SMA connectors (E.F. Johnson 142-0701-631 or equivalent), a high-Q capacitor (ATC 100A101MCA50 or equivalent), miscellaneous hardware and an HSMS-286B are added to create the test circuit shown in Figure 16.

The calculated input impedance for this network is shown in Figure 17.

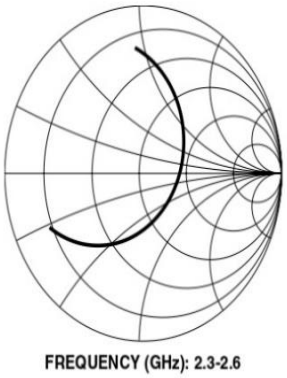


Figure 17. Input Impedance, 3 µA Bias.

The corresponding input match is shown in Figure 18. As was the case with the lower frequency design, bandwidth is more than adequate for the intended RFID application.

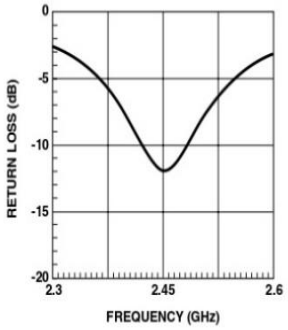


Figure 18. Input Return Loss, 3 µA Bias.

A word of caution to the designer is in order. A glance at Figure 17 will reveal the fact that the circuit does not provide the optimum impedance to the diode at 2.45 GHz. The temptation will be to adjust the circuit elements to achieve an ideal single frequency match, as illustrated in Figure 19.

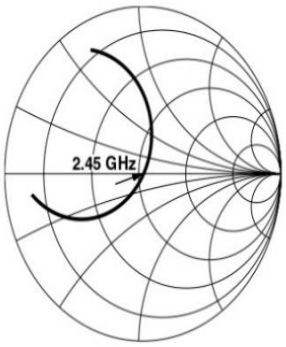


Figure 19. Input Impedance. Modified 2.45 GHz Circuit.

This does indeed result in a very good match at midband, as shown in Figure 20.

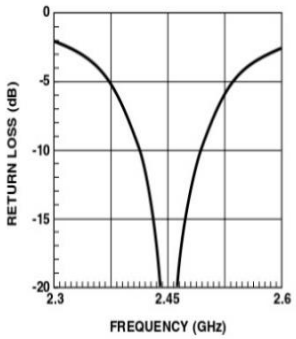


Figure 20. Input Return Loss. Modified 2.45 GHz Circuit.

However, bandwidth is narrower and the designer runs the risk of a shift in the midband frequency of his circuit if there is any small deviation in circuit board or diode characteristics due to lot-to-lot variation or change in temper-ature. The matching technique illustrated in Figure 17 is much less sensitive to changes in diode and circuit board processing.

5.8 GHz Detector Circuit

A possible design for a 5.8 GHz detector is given in Figure 21.

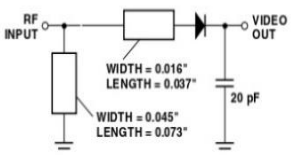


Figure 21. 5.8 GHz Matching Network for the HSMS-286x Series at 3 µA Bias.

As was the case at 2.45 GHz, the circuit is entirely distributed element, both low cost and compact. Input impedance for this network is given in Figure 22.

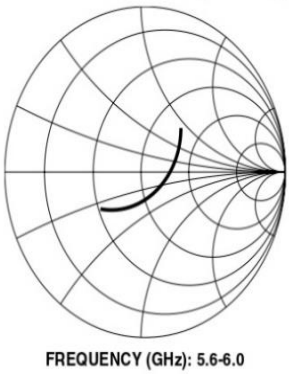


Figure 22. Input Impedance.

Input return loss, shown in Figure 23, exhibits wideband match.

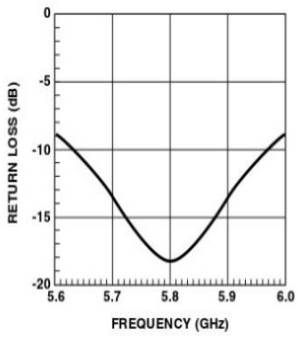


Figure 23. Input Return Loss.

Voltage Doublers

To this point, we have restricted our discussion to single diode detectors. A glance at Figure 9, however, will lead to the suggestion that the two types of single diode detectors be combined into a two diode voltage doubler[4] (known also as a full wave rectifier). Such a detector is shown in Figure 24.

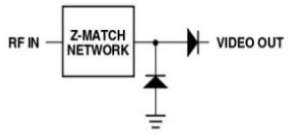


Figure 24. Voltage Doubler Circuit.

Such a circuit offers several advantages. First the voltage outputs of two diodes are added in series, increasing the overall value of voltage sensitivity for the network (compared to a single diode detector). Second, the RF impedances of the two diodes are added in parallel, making the job of reactive matching a bit easier. Such a circuit can easily be realized using the two series diodes in the HSMS-286C.

The "Virtual Battery"

The voltage doubler can be used as a virtual battery, to provide power for the operation of an I.C. or a transistor oscillator in a tag. Illuminated by the CW signal from a reader or interrogator, the Schottky circuit will produce power sufficient to operate an I.C. or to charge up a capacitor for a burst transmission from an oscillator. Where such virtual batteries are employed, the bulk, cost, and limited lifetime of a battery are eliminated.

Temperature Compensation

The compression of the detector's transfer curve is beyond the scope of this data sheet, but some general comments can be made. As was given earlier, the diode's video resistance is given by

$$R_V = \frac{8.33 \times 10^{-5}\, nT}{I_s + I_b}$$

where T is the diode's temperature in °K.

As can be seen, temperature has a strong effect upon R_V, and this will in turn affect video bandwidth and input RF impedance. A glance at Figure 6 suggests that the proper choice of bias current in the HSMS-286x series can minimize variation over temperature.

The detector circuits described earlier were tested over temperature. The 915 MHz voltage doubler using the HSMS-286C series produced the output voltages as shown in Figure 25. The use of 3 µA of bias resulted in the highest voltage sensitivity, but at the cost of a wide variation over temperature. Dropping the bias to 1 µA produced a detector with much less temperature variation.

A similar experiment was conducted with the HSMS-286B series in the 5.8 GHz detector. Once again, reducing the bias to some level under 3 µA stabilized the output of the detector over a wide temperature range.

It should be noted that curves such as those given in Figures 25 and 26 are highly dependent upon the exact design of the input impedance matching network. The designer will have to experiment with bias current using his specific design.

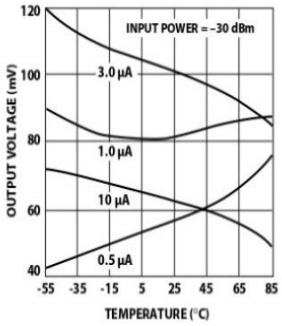


Figure 25. Output Voltage vs. Temperature and Bias Current in the 915 MHz Voltage Doubler using the HSMS-286C.

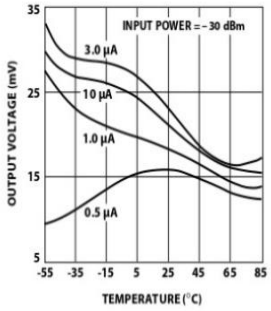


Figure 26. Output Voltage vs. Temperature and Bias Current in the 5.80 GHz Voltage Detector using the HSMS-286B Schottky.

Six Lead Circuits

The differential detector is often used to provide temperature compensation for a Schottky detector, as shown in Figures 27 and 28.

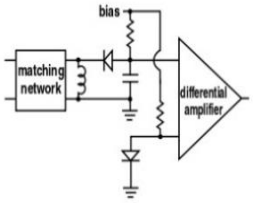


Figure 27. Differential Detector.

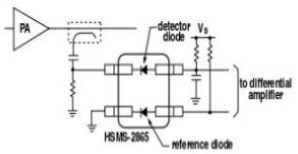


Figure 28. Conventional Differential Detector.

These circuits depend upon the use of two diodes having matched V_f characteristics over all operating temperatures. This is best achieved by using two diodes in a single package, such as the SOT-143 HSMS-2865 as shown in Figure 29.

In high power differential detectors, RF coupling from the detector diode to the reference diode produces a rectified voltage in the latter, resulting in errors.

Isolation between the two diodes can be obtained by using the HSMS-286K diode with leads 2 and 5 grounded. The difference between this product and the conventional HSMS-2865 can be seen in Figure 29.

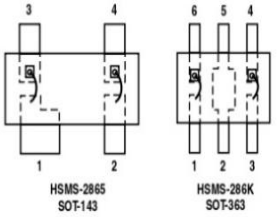


Figure 29. Comparing Two Diodes.

The HSMS-286K, with leads 2 and 5 grounded, offers some isolation from RF coupling between the diodes. This product is used in a differential detector as shown in Figure 30.

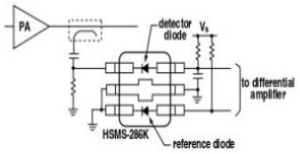


Figure 30. High Isolation Differential Detector.

In order to achieve the maximum isolation, the designer must take care to minimize the distance from leads 2 and 5 and their respective ground via holes.

Tests were run on the HSMS-282K and the conventional HSMS-2825 pair, which compare with each other in the same way as the HSMS-2865 and HSMS-286K, with the results shown in Figure 31.

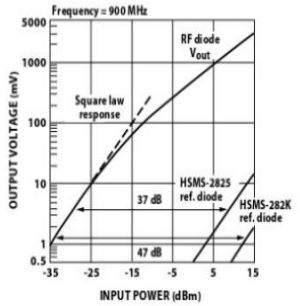


Figure 31. Comparing HSMS-282K with HSMS-2825.

The line marked "RF diode, V_{out}" is the transfer curve for the detector diode—both the HSMS-2825 and the HSMS-282K exhibited the same output voltage. The data were taken over the 50 dB dynamic range shown. To the right is the output voltage (transfer) curve for the reference diode of the HSMS-2825, showing 37 dB of isolation. To the right of that is the output voltage due to RF leakage for the reference diode of the HSMS-282K, demonstrating 10 dB higher isolation than the conventional part.

Such differential detector circuits generally use single diode detectors, either series or shunt mounted diodes. The voltage doubler offers the advantage of twice the output voltage for a given input power. The two concepts can be combined into the differential voltage doubler, as shown in Figure 32.

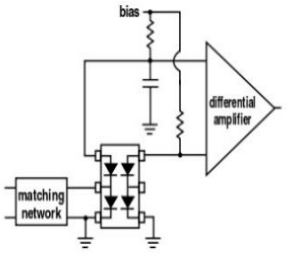


Figure 32. Differential Voltage Doubler, HSMS-286P.

Here, all four diodes of the HSMS-286P are matched in their V_f characteristics, because they came from adjacent sites on the wafer. A similar circuit can be realized using the HSMS-286R ring quad.

Other configurations of six lead Schottky products can be used to solve circuit design problems while saving space and cost.

Thermal Considerations

The obvious advantage of the SOT-363 over the SOT-143 is combination of smaller size and two extra leads. However, the copper leadframe in the SOT-323 and SOT-363 has a thermal conductivity four times higher than the Alloy 42 leadframe of the SOT-23 and SOT-143, which enables it to dissipate more power.

The maximum junction temperature for these three families of Schottky diodes is 150°C under all operating conditions. The following equation, equation 1, applies to the thermal analysis of diodes:

$$T_j = (V_f I_f + P_{RF})\,\theta_{jc} + T_a \qquad \text{Equation (1).}$$

where

T_j = junction temperature

T_a = diode case temperature

θ_{jc} = thermal resistance

$V_f I_f$ = DC power dissipated

P_{RF} = RF power dissipated

Note that θ_{jc}, the thermal resistance from diode junction to the foot of the leads, is the sum of two component resistances,

$$\theta_{jc} = \theta_{pkg} + \theta_{chip} \qquad \text{Equation (2).}$$

Package thermal resistance for the SOT-323 and SOT-363 package is approximately 100°C/W, and the chip thermal resistance for these three families of diodes is approximately 40°C/W. The designer will have to add in the thermal resistance from diode case to ambient—a poor choice of circuit board material or heat sink design can make this number very high.

Equation (1) would be straightforward to solve but for the fact that diode forward voltage is a function of temperature as well as forward current. The equation, equation 3, for V_f is:

$$I_f = I_S\left[e^{\frac{11600\,(V_f - I_f R_s)}{nT}} - 1\right] \qquad \text{Equation (3).}$$

where

n = ideality factor

T = temperature in °K

R_s = diode series resistance

and I_S (diode saturation current) is given by

$$I_s = I_0\left(\frac{T}{298}\right)^{\frac{2}{n}} e^{-4060\left(\frac{1}{T} - \frac{1}{298}\right)} \qquad \text{Equation (4).}$$

Equations (1) and (3) are solved simultaneously to obtain the value of junction temperature for given values of diode case temperature, DC power dissipation and RF power dissipation.

Diode Burnout

Any Schottky junction, be it an RF diode or the gate of a MESFET, is relatively delicate and can be burned out with excessive RF power. Many crystal video receivers used in RFID (tag) applications find themselves in poorly controlled environments where high power sources may be present. Examples are the areas around airport and FAA radars, nearby ham radio operators, the vicinity of a broadcast band transmitter, etc. In such environments, the Schottky diodes of the receiver can be protected by a device known as a limiter diode.[6] Formerly available only in radar warning receivers and other high cost electronic warfare applications, these diodes have been adapted to commercial and consumer circuits.

Avago offers a complete line of surface mountable PIN limiter diodes. Most notably, our HSMP-4820 (SOT-23) or HSMP-482B (SOT-323) can act as a very fast (nano-second) power-sensitive switch when placed between the antenna and the Schottky diode, shorting out the RF circuit temporarily and reflecting the excessive RF energy back out the antenna.

Assembly Instructions

SOT-323 PCB Footprint

A recommended PCB pad layout for the miniature SOT-323 (SC-70) package is shown in Figure 33 (dimensions are in inches).

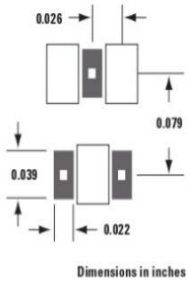


Figure 33. Recommended PCB Pad Layout for Avago's SC70 3L/SOT-323 Products.

A recommended PCB pad layout for the miniature SOT-363 (SC-70 6 lead) package is shown in Figure 34 (dimensions are in inches). This layout provides ample allowance for package placement by automated assembly equipment without adding parasitics that could impair the performance.

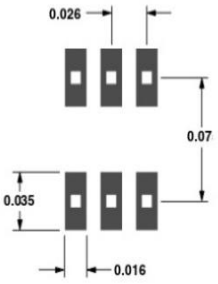


Figure 34. Recommended PCB Pad Layout for Avago's SC70 6L/SOT-363 Products.

[6] Avago Application Note 1050, Low Cost, Surface Mount Power Limiters.

SMT Assembly

Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g., IR or vapor phase reflow, wave soldering, etc.) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the SOT packages, will reach solder reflow temperatures faster than those with a greater mass.

Avago's diodes have been qualified to the time-temperature profile shown in Figure 35. This profile is representative of an IR reflow type of surface mount assembly process.

After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat zones. The preheat zones increase the temperature of the board and components to prevent thermal shock and begin evaporating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

The rates of change of temperature for the ramp-up and cool-down zones are chosen to be low enough to not cause deformation of the board or damage to components due to thermal shock. The maximum temperature in the reflow zone (T_{MAX}) should not exceed 260°C.

These parameters are typical for a surface mount assembly process for Avago diodes. As a general guideline, the circuit board and components should be exposed only to the minimum temperatures and times necessary to achieve a uniform reflow of solder.

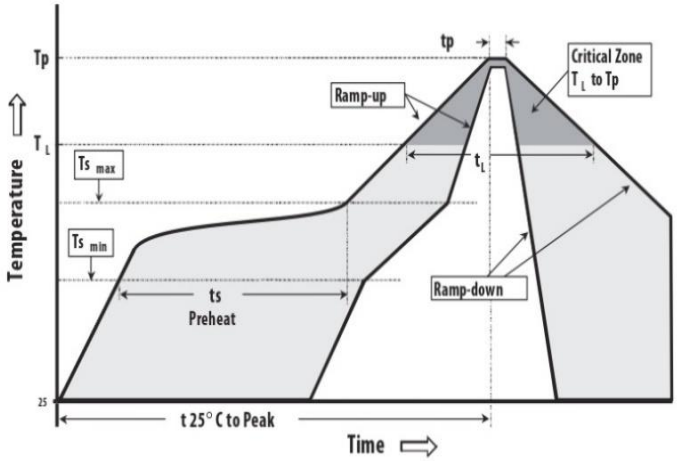


Figure 35. Surface Mount Assembly Profile.

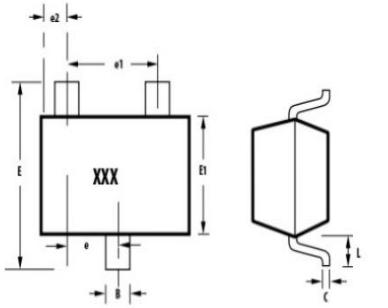
Lead-Free Reflow Profile Recommendation (IPC/JEDEC J-STD-020C)

Reflow Parameter		Lead-Free Assembly
Average ramp-up rate (Liquidus Temperature ($T_{S(max)}$ to Peak)		3°C/ second max
Preheat	Temperature Min ($T_{S(min)}$)	150°C
	Temperature Max ($T_{S(max)}$)	200°C
	Time (min to max) (t_S)	60-180 seconds
Ts(max) to TL Ramp-up Rate		3°C/second max
Time maintained above:	Temperature (T_L)	217°C
	Time (t_L)	60-150 seconds
Peak Temperature (T_P)		260 +0/-5°C
Time within 5 °C of actual Peak temperature (t_p)		20-40 seconds
Ramp-down Rate		6°C/second max
Time 25 °C to Peak Temperature		8 minutes max

Note 1: All temperatures refer to topside of the package, measured on the package body surface

Package Dimensions

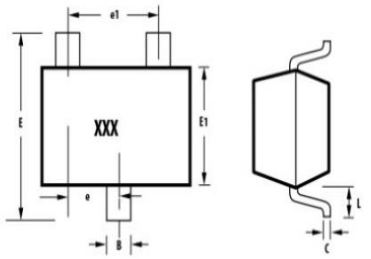
Outline 23 (SOT-23)



SYMBOL	DIMENSIONS (mm) MIN.	MAX.
A	0.79	1.20
A1	0.000	0.100
B	0.30	0.54
C	0.08	0.20
D	2.73	3.13
E1	1.35	1.50
e	0.89	1.02
e1	1.78	2.04
e2	0.45	0.60
E	2.10	2.70
L	0.45	0.69

Notes:
XXX-package marking
Drawings are not to scale

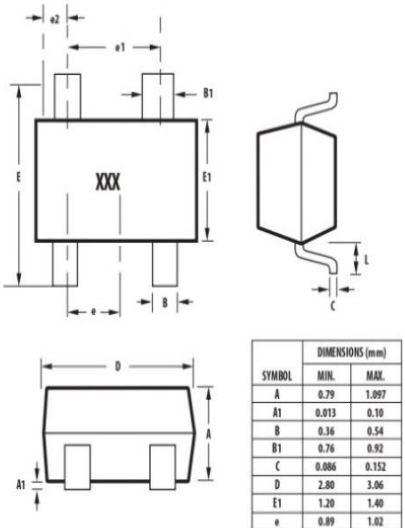
Outline SOT-323 (SC-70 3 Lead)



SYMBOL	DIMENSIONS (mm) MIN.	MAX.
A	0.80	1.00
A1	0.00	0.10
B	0.15	0.40
C	0.08	0.25
D	1.80	2.25
E1	1.30	1.40
e	0.65 typical	
e1	1.30 typical	
E	1.80	2.40
L	0.26	0.46

Notes:
XXX-package marking
Drawings are not to scale

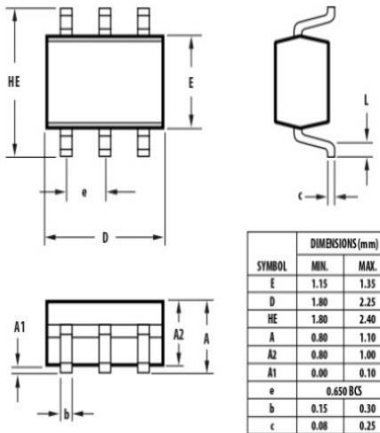
Outline 143 (SOT-143)



SYMBOL	DIMENSIONS (mm) MIN.	MAX.
A	0.79	1.097
A1	0.013	0.10
B	0.36	0.54
B1	0.76	0.92
C	0.086	0.152
D	2.80	3.06
E1	1.20	1.40
e	0.89	1.02
e1	1.78	2.04
e2	0.45	0.60
E	2.10	2.65
L	0.45	0.69

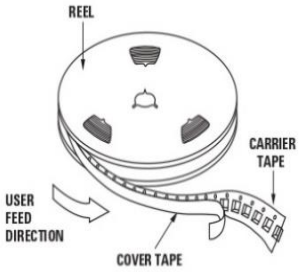
Notes:
XXX-package marking
Drawings are not to scale

Outline SOT-363 (SC-70 6 Lead)

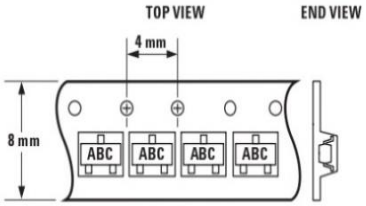


SYMBOL	DIMENSIONS (mm) MIN.	MAX.
E	1.15	1.35
D	1.80	2.25
HE	1.80	2.40
A	0.80	1.10
A2	0.80	1.00
A1	0.00	0.10
e	0.650 BCS	
b	0.15	0.30
c	0.08	0.25
L	0.10	0.46

Device Orientation

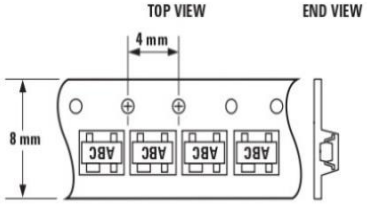


For Outlines SOT-23, -323



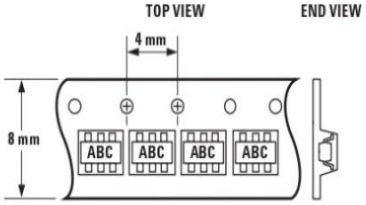
Note: "AB" represents package marking code.
"C" represents date code.

For Outline SOT-143



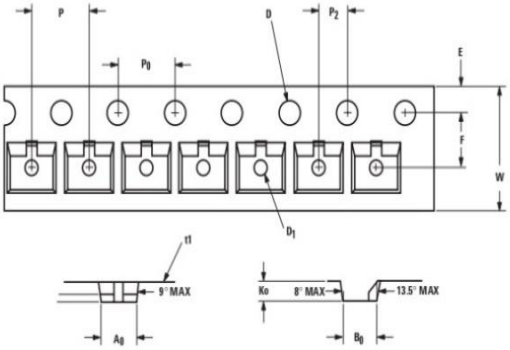
Note: "AB" represents package marking code.
"C" represents date code.

For Outline SOT-363



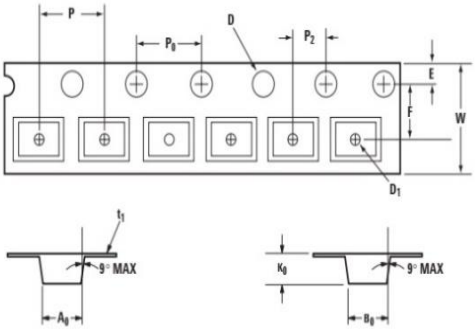
Note: "AB" represents package marking code.
"C" represents date code.

Tape Dimensions and Product Orientation
For Outline SOT-23



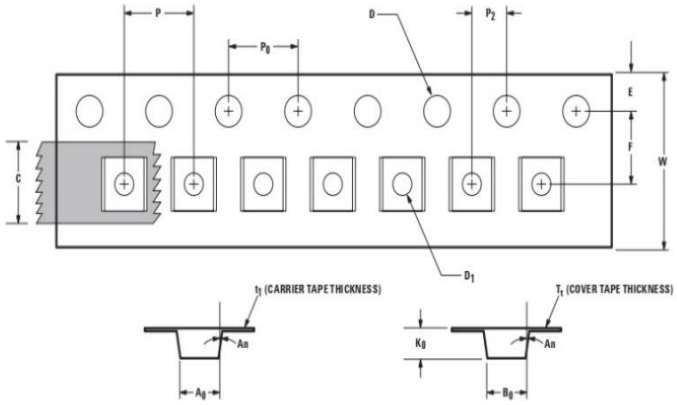
DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	3.15 ± 0.10	0.124 ± 0.004
	WIDTH	B_0	2.77 ± 0.10	0.109 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.05	0.039 ± 0.002
PERFORATION	DIAMETER	D	1.50 + 0.10	0.059 + 0.004
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00+0.30–0.10	0.315+0.012–0.004
	THICKNESS	t1	0.229 ± 0.013	0.009 ± 0.0005
DISTANCE BETWEEN CENTERLINE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

For Outline SOT-143



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	3.19 ± 0.10	0.126 ± 0.004
	WIDTH	B_0	2.80 ± 0.10	0.110 ± 0.004
	DEPTH	K_0	1.31 ± 0.10	0.052 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.50 + 0.10	0.059 + 0.004
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 +0.30–0.10	0.315+0.012–0.004
	THICKNESS	t1	0.254 ± 0.013	0.0100 ± 0.0005
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

Tape Dimensions and Product Orientation
For Outlines SOT-323, -363



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.40 ± 0.10	0.094 ± 0.004
	WIDTH	B_0	2.40 ± 0.10	0.094 ± 0.004
	DEPTH	K_0	1.20 ± 0.10	0.047 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.254 ± 0.02	0.0100 ± 0.0008
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002
ANGLE	FOR SOT-323 (SC70-3 LEAD)	An	8°C MAX	
	FOR SOT-363 (SC70-6 LEAD)		10°C MAX	

Part Number Ordering Information

Part Number	No. of Devices	Container
HSMS-286x-TR2G	10000	13" Reel
HSMS-286x-TR1G	3000	7" Reel
HSMS-286x-BLKG	100	antistatic bag

where x = 0, 2, 3, 4, 5, B, C, E, F, K, L, P or R for HSMS-286x.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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AVAGO TECHNOLOGIES

RESUME

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